

SYSTEM BLOCK DIAGRAM

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[illegible][illegible]

POWER SYSTEM ARCHITECTURE

The diagram illustrates the power management system, showing the flow of power from the AC Adapter (PG 30) and Backup Battery (PG 31) through various regulators and sequencers to the system components.

Power Sources and Initial Regulation:

- AC ADAPTER IN (PG 30):** Provides input to the INRUSH LIMITER (PG 30) and the +3V_PMU LDO (PG 31).
- BACKUP BATTERY (PG 31):** Provides input to the +3V_PMU LDO (PG 31) and the CHARGER INPUT & BOOST OUTPUT (PG 31).
- CHARGER INPUT & BOOST OUTPUT (PG 31):** Provides input to the BATTERY CHARGER (MAX1772) (PG 30).
- 3S 2P 18650 CELLS:** Provides input to the BATTERY VOLTAGE FEED-IN PATH (PG 30).

Regulators and Sequencers:

- INRUSH LIMITER (PG 30):** Limits inrush current from the AC adapter.
- +3V_PMU LDO (PG 31):** Regulates the 3V PMU supply.
- BATTERY CHARGER (MAX1772) (PG 30):** Charges the backup battery.
- BATTERY VOLTAGE FEED-IN PATH (PG 30):** Provides a feed-in path for the battery voltage.
- BUCK REGULATOR (LTC1625) (PG 31):** Regulates the +24V_PBUS supply.
- DC/DC (LTC3707) (PG 32):** Regulates the +5V_MAIN supply.
- DC/DC (LTC3411) (PG 34):** Regulates the +1.8V_MAIN supply.
- DC/DC (MAX1715) (PG 34):** Regulates the +2.5V_MAIN and +1.5V_MAIN supplies.
- DC/DC (MAX1717) (PG 33):** Regulates the CPU_VCORE (+1.385V) and GPU_VCORE (+1.2V) supplies.

Control and Sequencing:

- MAXBUS SEQUENCING:** Controls the MAXBUS signal.
- GPU_VCORE SEQUENCING:** Controls the GPU_VCORE signal.
- DCDC_EN, DCDC_EN_L, DCDC_EN_H:** Control signals for the DC/DC converters.
- 1_5V_2_5V_OK:** Status signal for the +2.5V_MAIN and +1.5V_MAIN supplies.
- 3V_5V_OK:** Status signal for the +5V_MAIN supply.

Timing Diagram:

The timing diagram shows the sequence of power transitions during SHUT-DOWN, RUN, SLEEP, and SHUT-DOWN. Key signals and their timing are:

- SLEEP:** SLEEP_L_LSE, DCDC_EN, DCDC_EN_L, +5V_MAIN, +5V_SLEEP, +3V_MAIN, +3V_SLEEP, 3V_5V_OK, +2_5V_MAIN, +2_5V_SLEEP, +1_5V_MAIN, +1_5V_SLEEP.
- RUN:** +5V_MAIN turns on ~2.23MS after DCDC_EN_L or PMU_POWERUP_L becomes '1'. +3V_MAIN turns on ~7.36MS after DCDC_EN_L or PMU_POWERUP_L becomes '1'. +2_5V_MAIN turns on ~2.4V - ??? MS after DCDC_EN_L or PMU_POWERUP_L becomes '1'. +1_5V_MAIN turns on ~8.2MS after DCDC_EN_L or PMU_POWERUP_L becomes '1'. GPU_VCORE turns on ~8.2MS after DCDC_EN_L or PMU_POWERUP_L becomes '1'.
- SLEEP:** SLEEP_L_LSE, DCDC_EN, DCDC_EN_L, +5V_MAIN, +5V_SLEEP, +3V_MAIN, +3V_SLEEP, 3V_5V_OK, +2_5V_MAIN, +2_5V_SLEEP, +1_5V_MAIN, +1_5V_SLEEP.
- SHUT-DOWN:** SLEEP_L_LSE, DCDC_EN, DCDC_EN_L, +5V_MAIN, +5V_SLEEP, +3V_MAIN, +3V_SLEEP, 3V_5V_OK, +2_5V_MAIN, +2_5V_SLEEP, +1_5V_MAIN, +1_5V_SLEEP.

POWER BLOCK DIAGRAM

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SIZE: D, DRAWING NUMBER: 051-6809, REV: B

SCALE: NONE, SHT: 3 OF 44

D

C

B

A

D

C

B

A

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

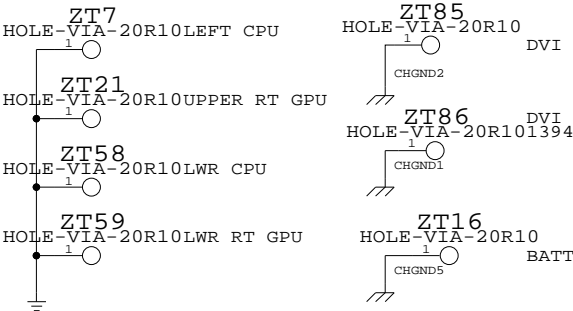
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA				SIGNAL (1/2 OZ + COPPER PLATING)	
1				SIGNAL (1/2 OZ)	
2	PREPREG (3 MIL)				
3	PREPREG (3 MIL)			GROUND (1/2 OZ)	
4	CORE (3 MIL)			SIGNAL (1/2 OZ)	
5	PREPREG (5 MIL)			CUT POWER PLANE (1 OZ)	
6	CORE (5 MIL)			CUT POWER PLANE (1 OZ)	
7	PREPREG (5 MIL)			SIGNAL (1/2 OZ)	
8	CORE (3 MIL)			GROUND (1/2 OZ)	
9	PREPREG (3 MIL)			SIGNAL (1/2 OZ)	
10	PREPREG (3 MIL)			SIGNAL (1/2 OZ + COPPER PLATING)	

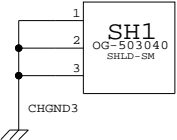
BOARD HOLES

CHASSIS MOUNTS

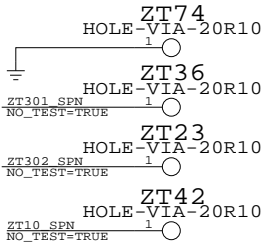
ASICS HEATSINK MOUNTS I/O AREA



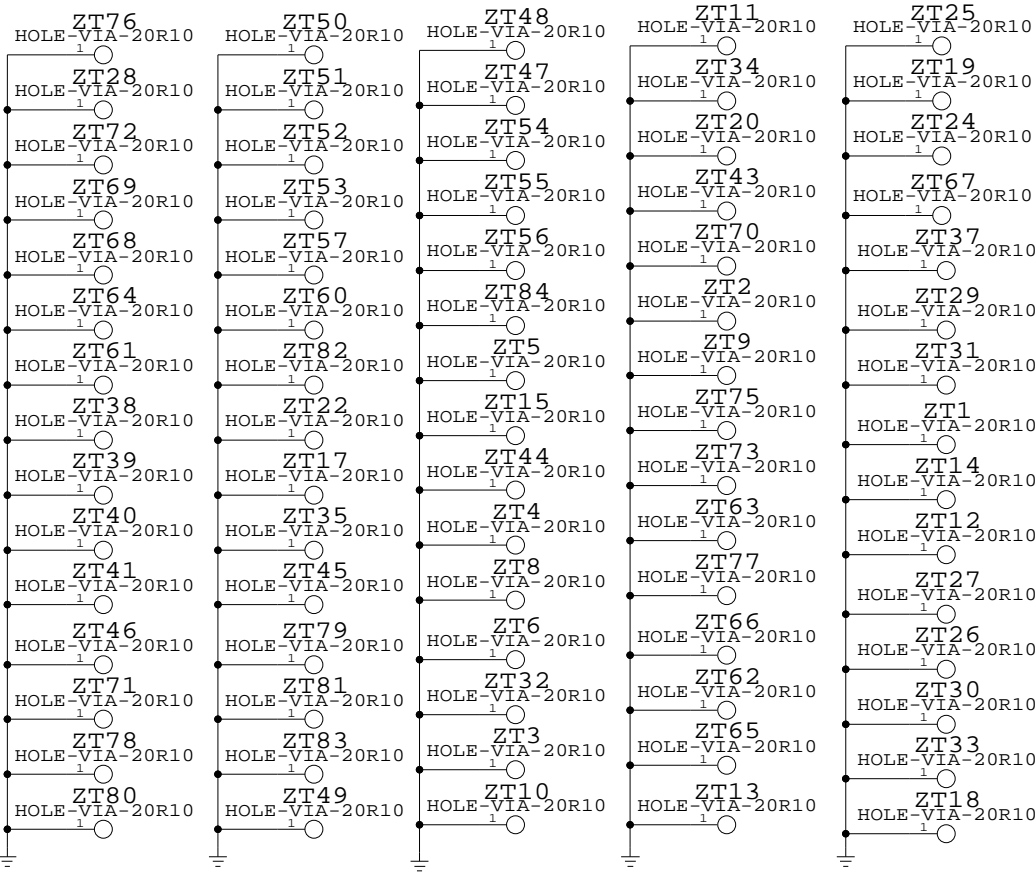
INVERTER



MECH. HOLES



GROUND VIAS



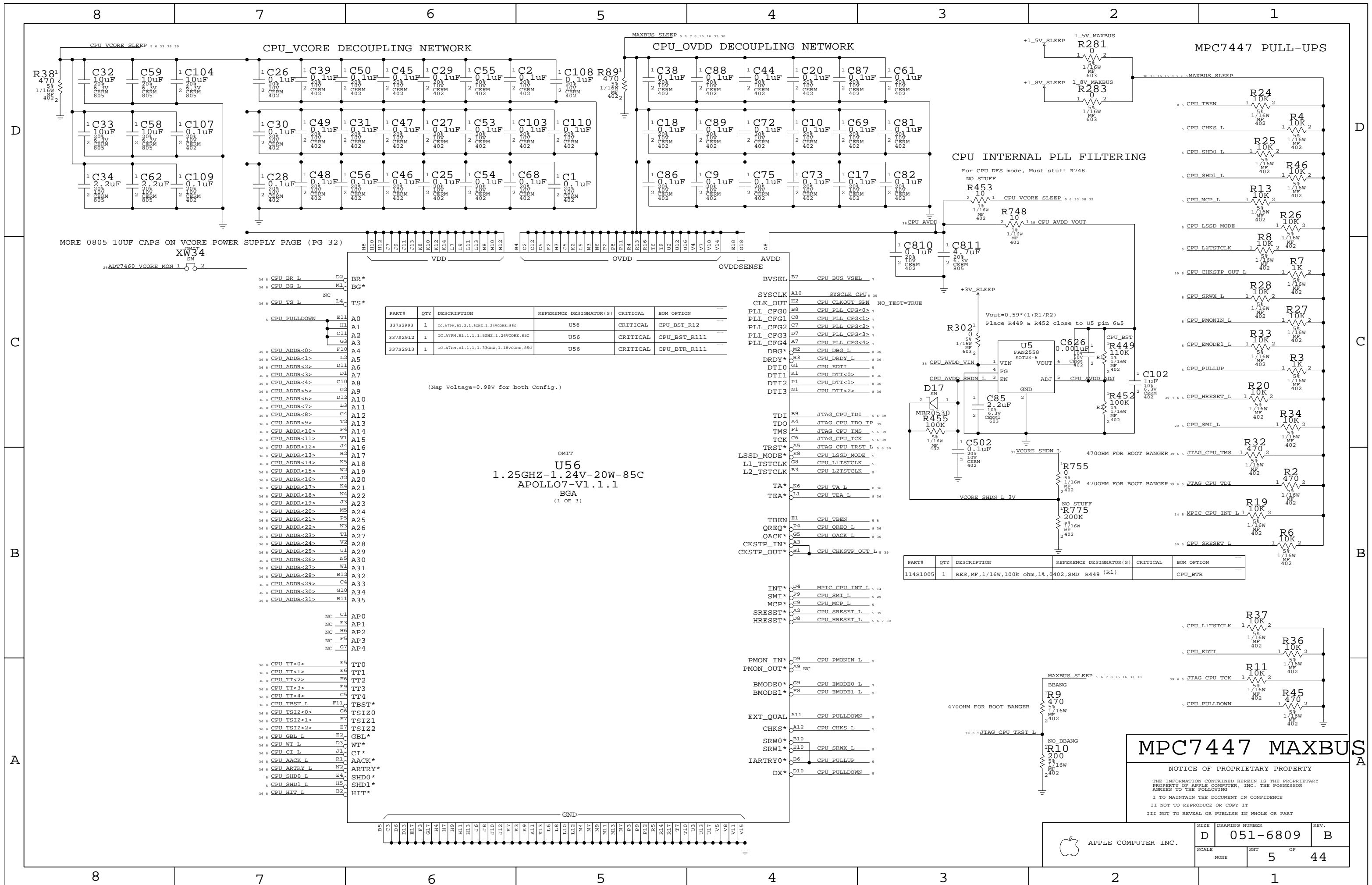
BOARD INFORMATION

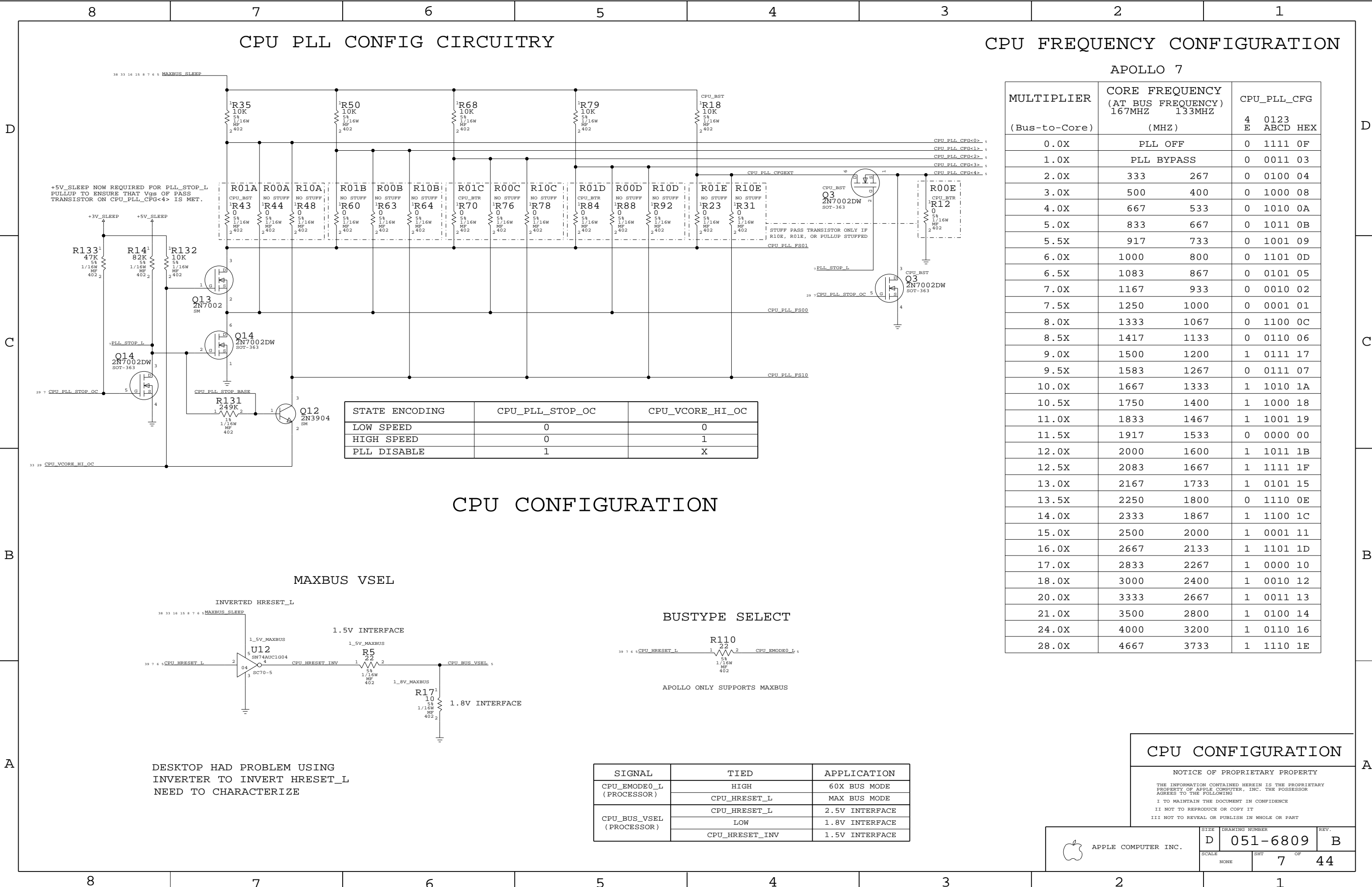
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SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	4	44





INTREPID BOOT STRAPS

BIT 32 TO 39

BIT 40 TO 47

BIT 48 TO 55

BIT 56 TO 63

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS

INTrepid MaxBus

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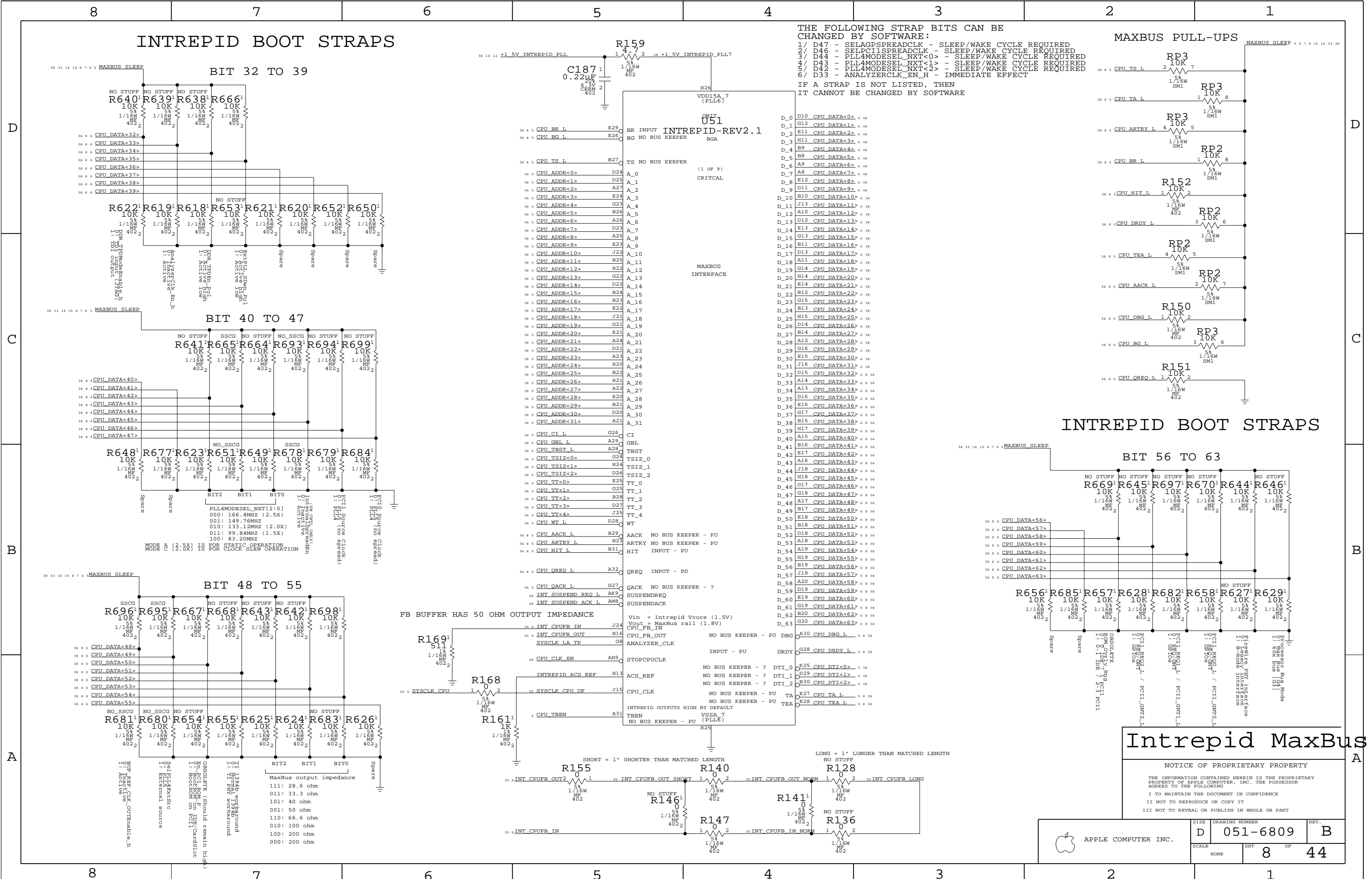
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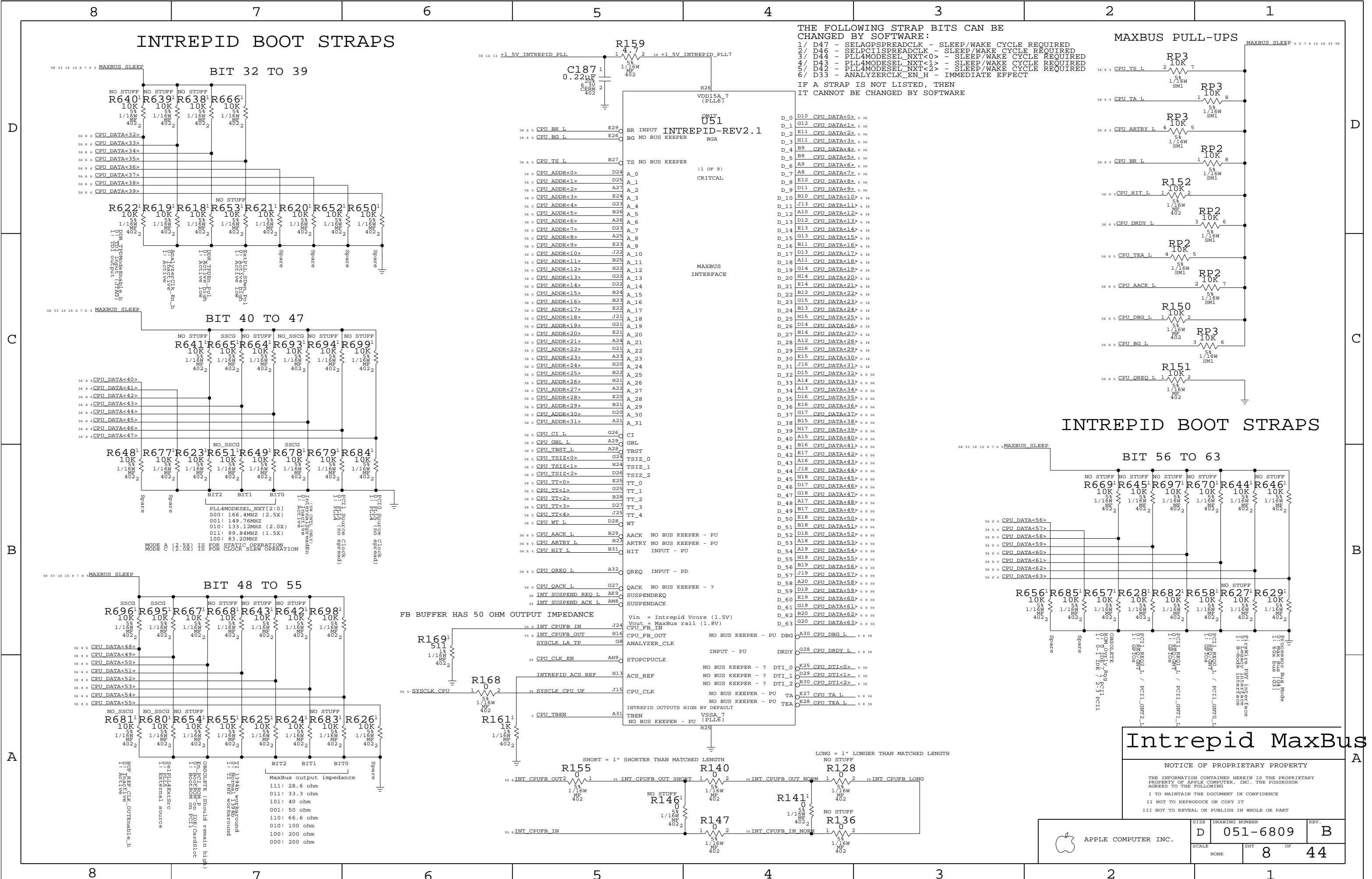
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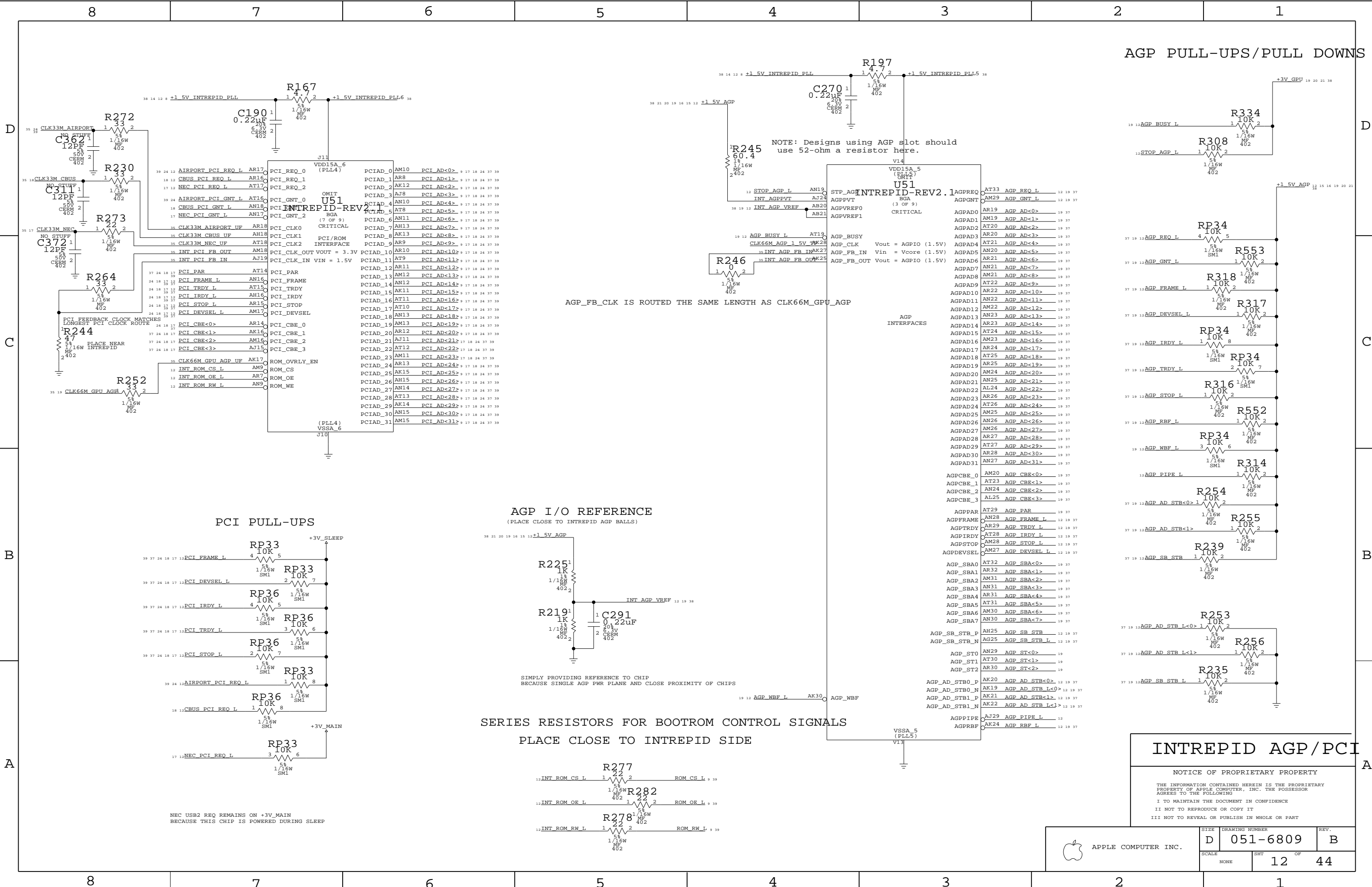
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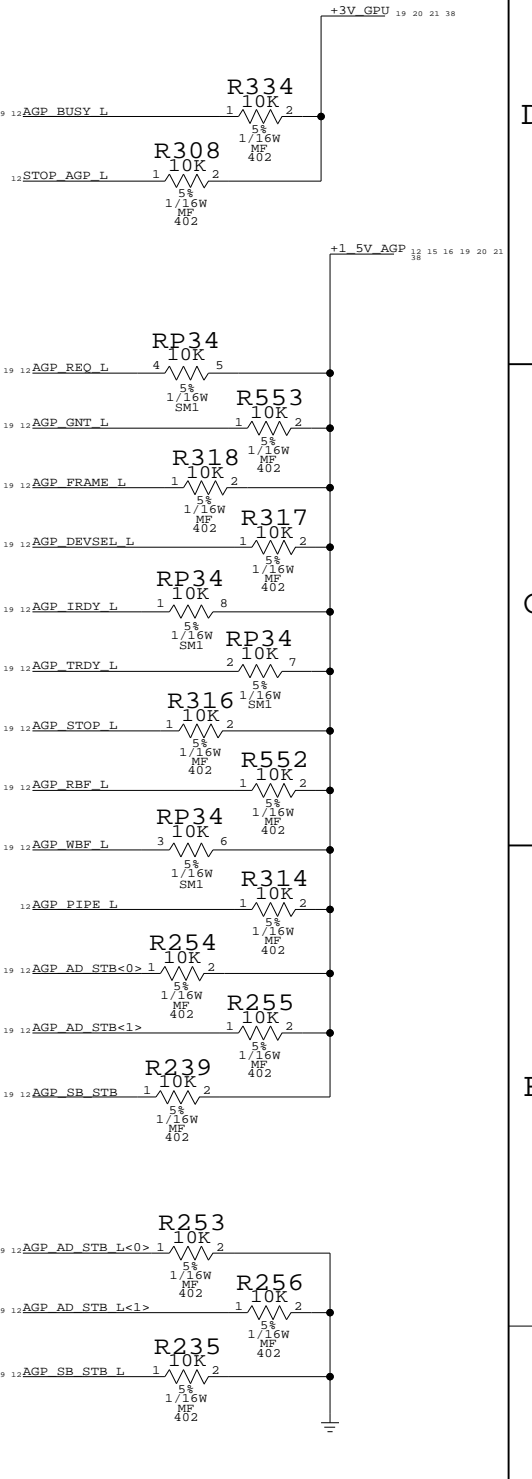
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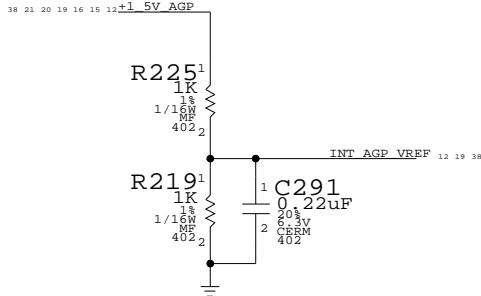


AGP PULL-UPS/PULL DOWNS



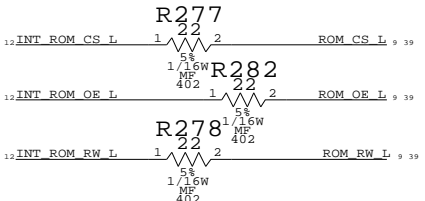
AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP

AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)

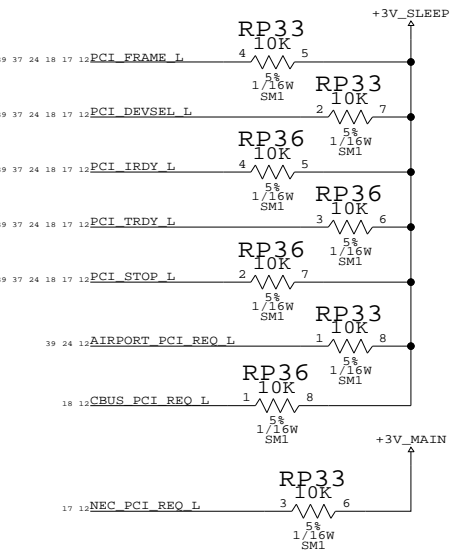


SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE



PCI PULL-UPS



NEC USB2 REQ REMAINS ON +3V_MAIN
BECAUSE THIS CHIP IS POWERED DURING SLEEP

INTREPID AGP/PCI

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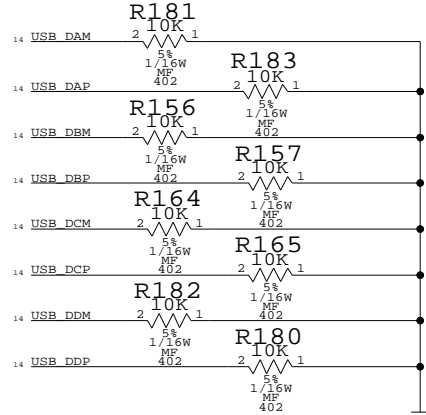


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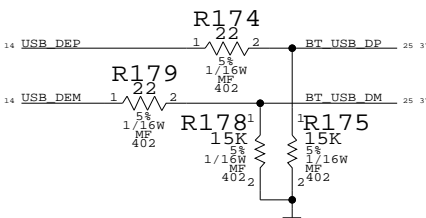
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USB PORT ASSIGNMENTS

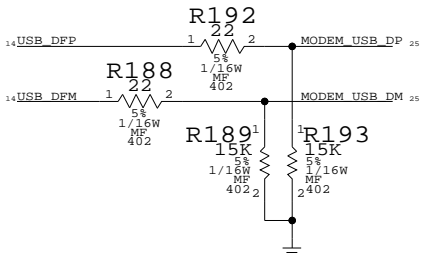
PORT A - PORT D/UNUSED



PORT E/BLUETOOTH



PORT F/MODEM

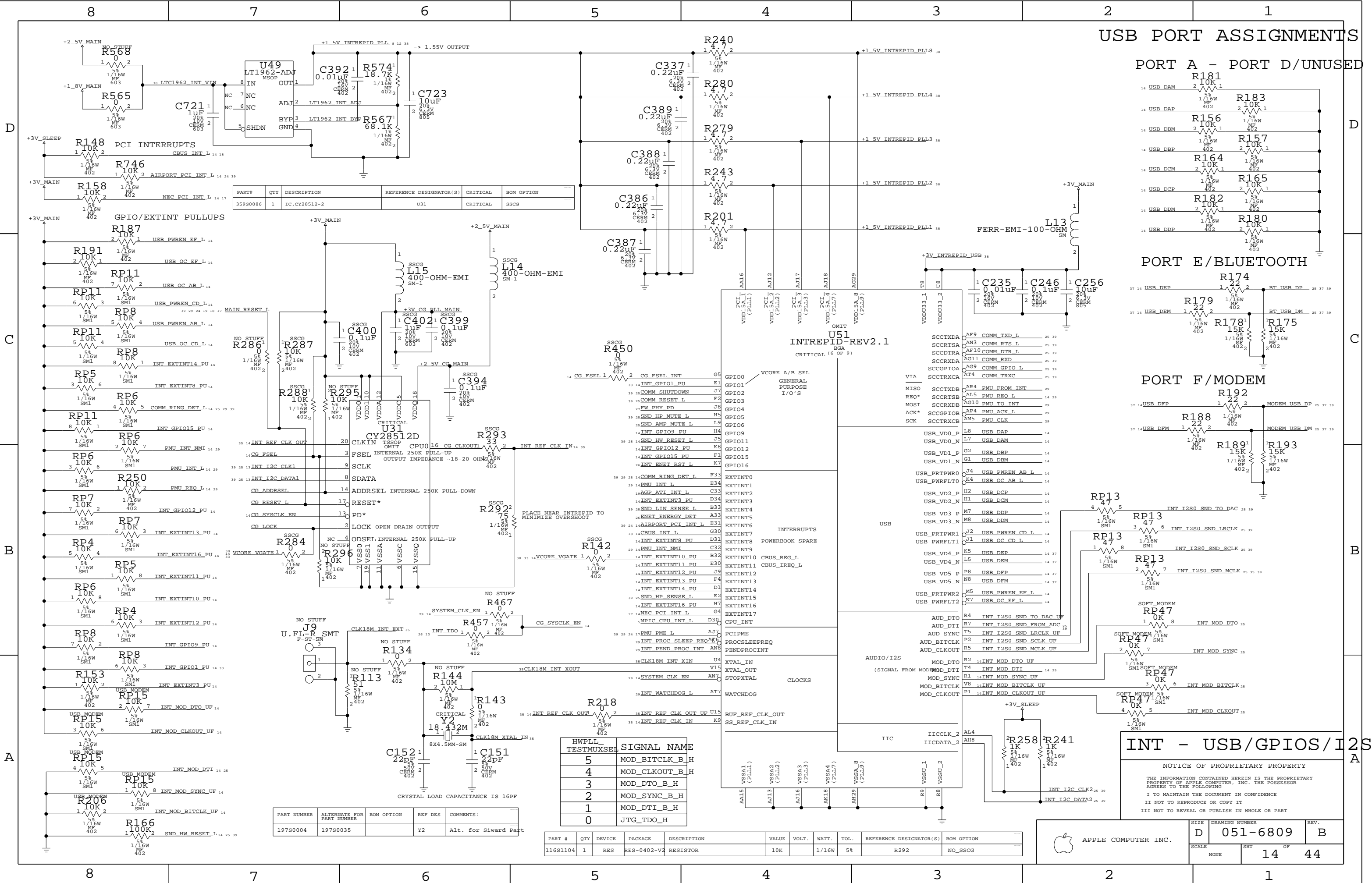


INT - USB/GPIOS/I2S

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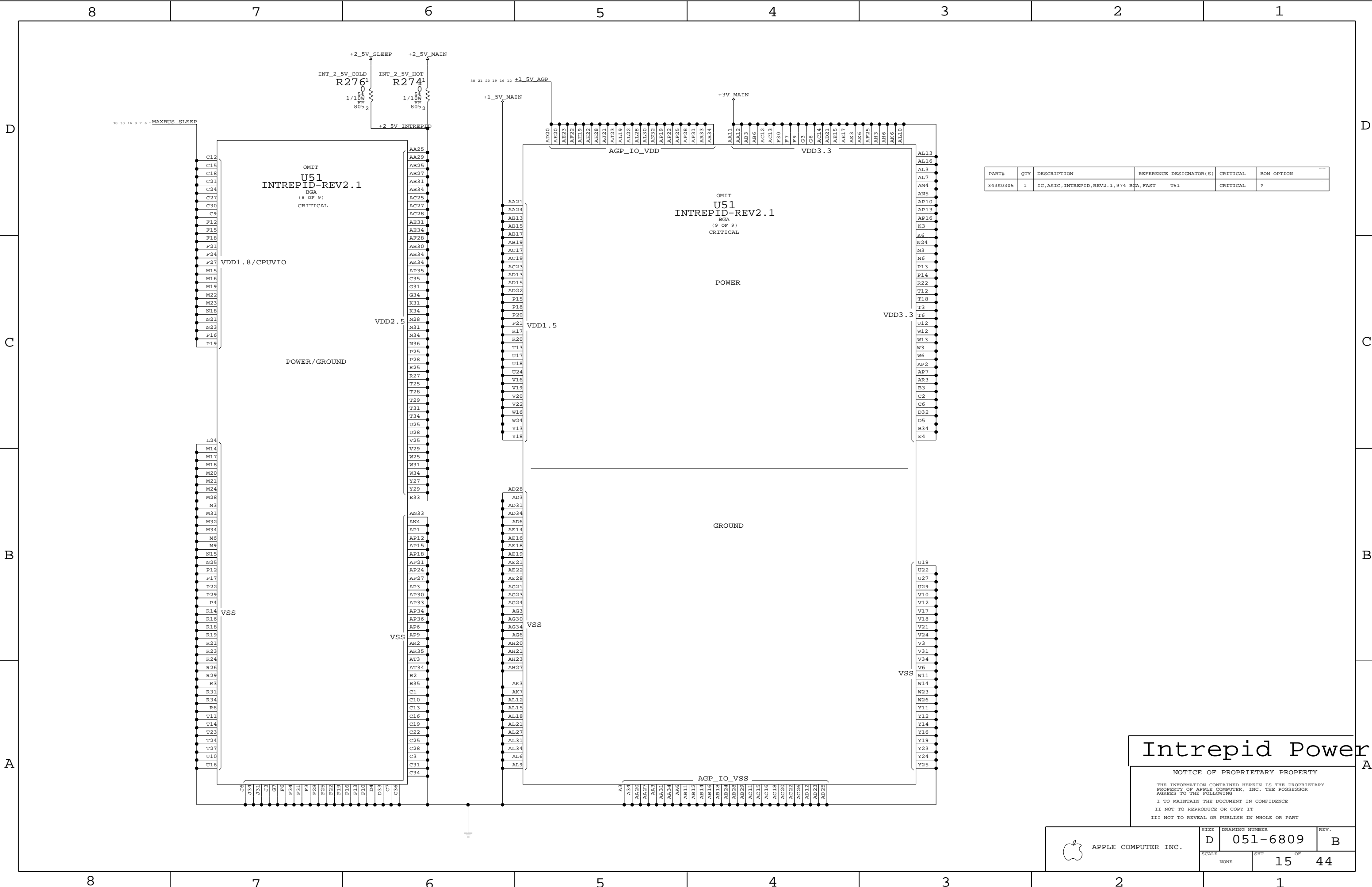


HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y2	Alt. for Siward Part



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974 BGA,FAST	U51	CRITICAL	?

Intrepid Power

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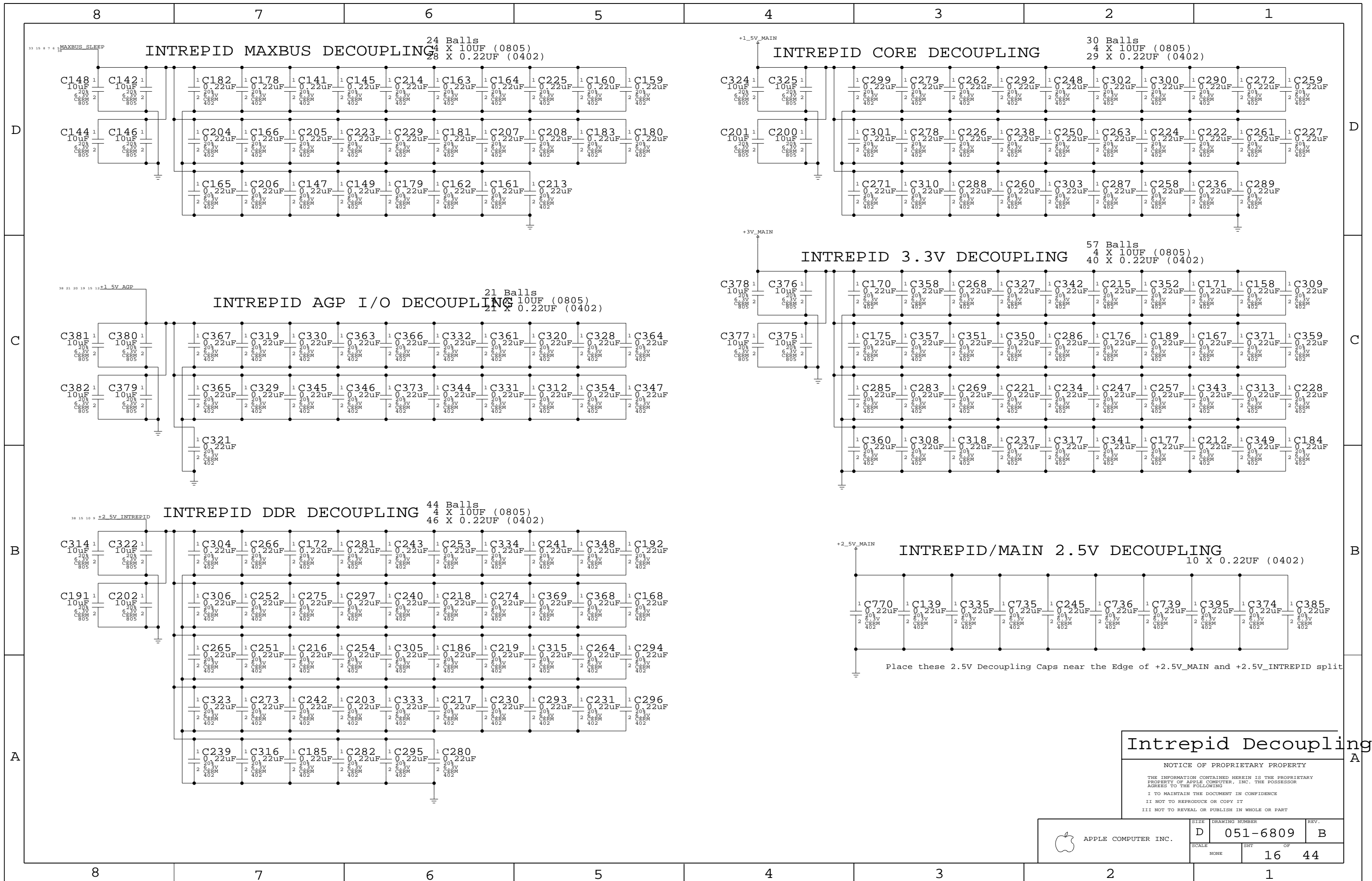
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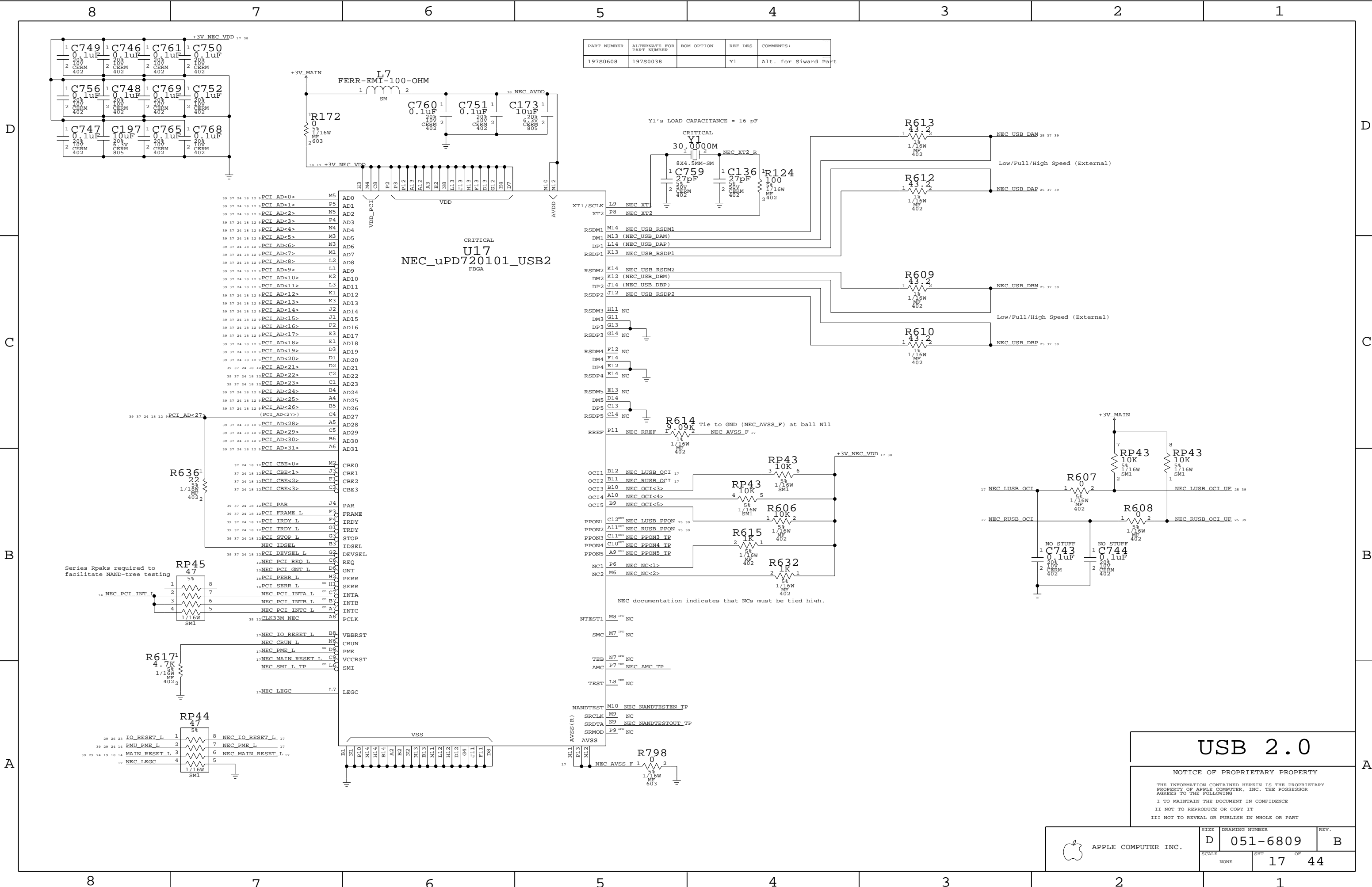


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USB 2.0

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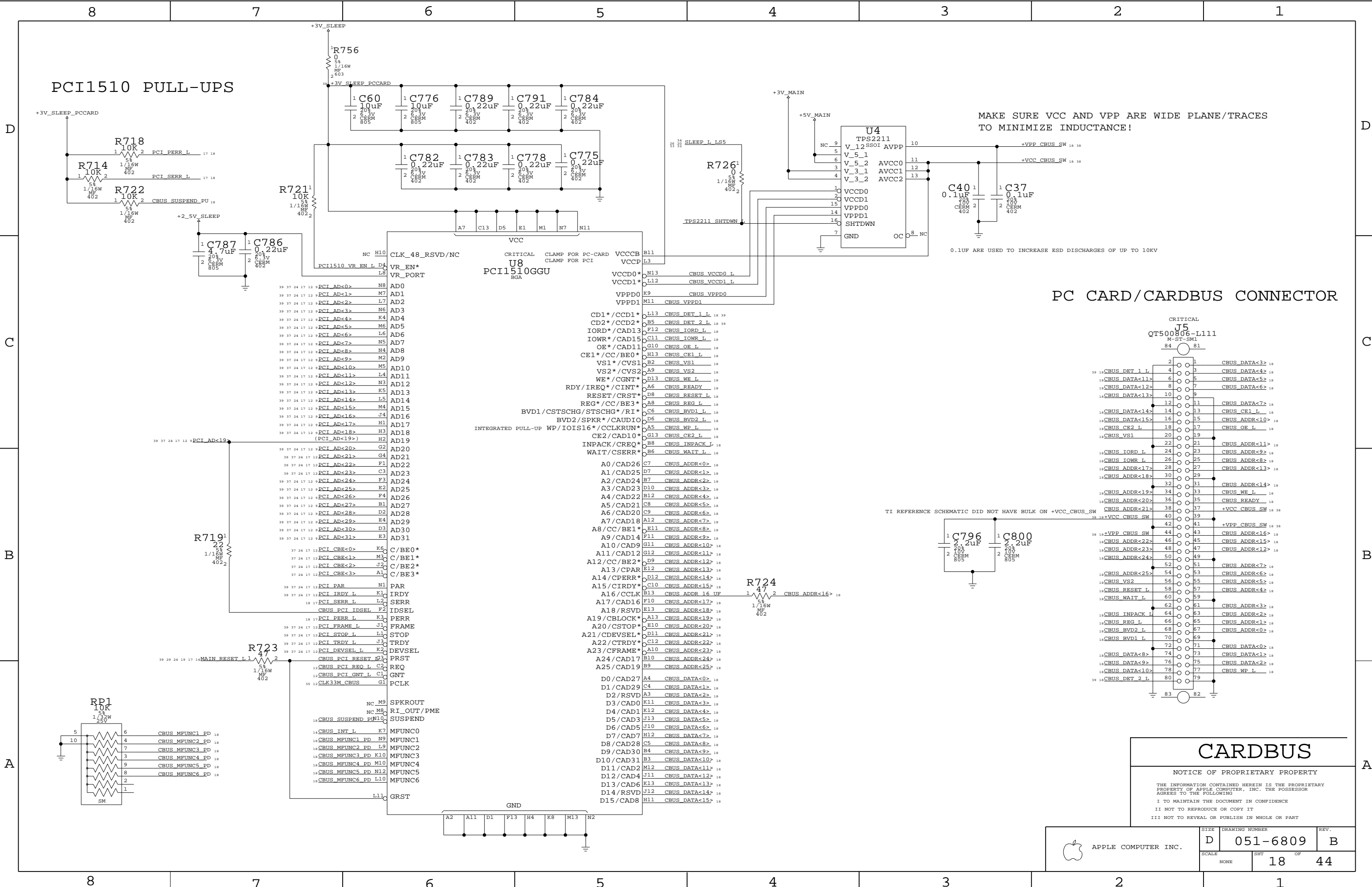


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PC CARD/CARDBUS CONNECTOR

CARDBUS


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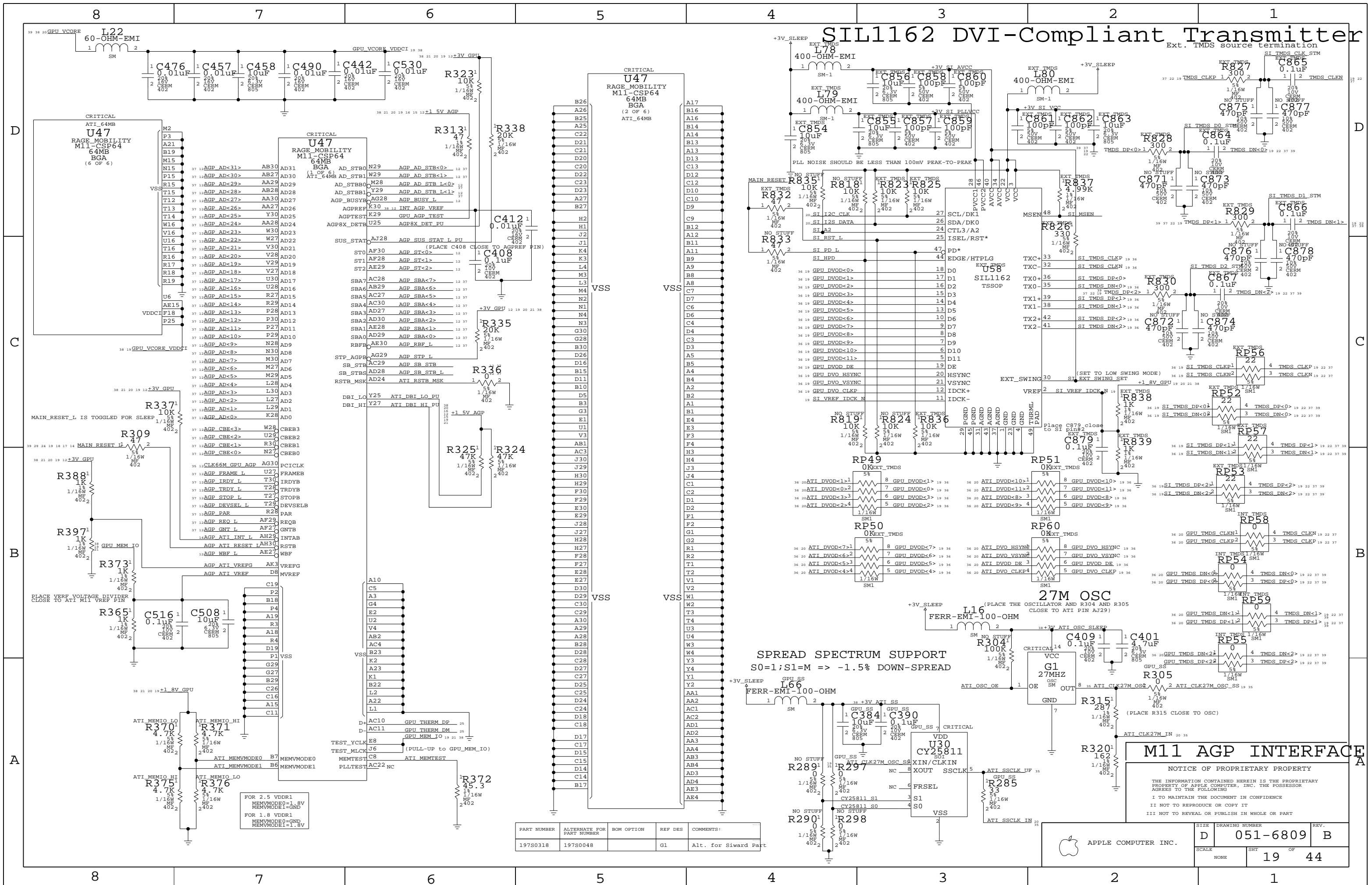
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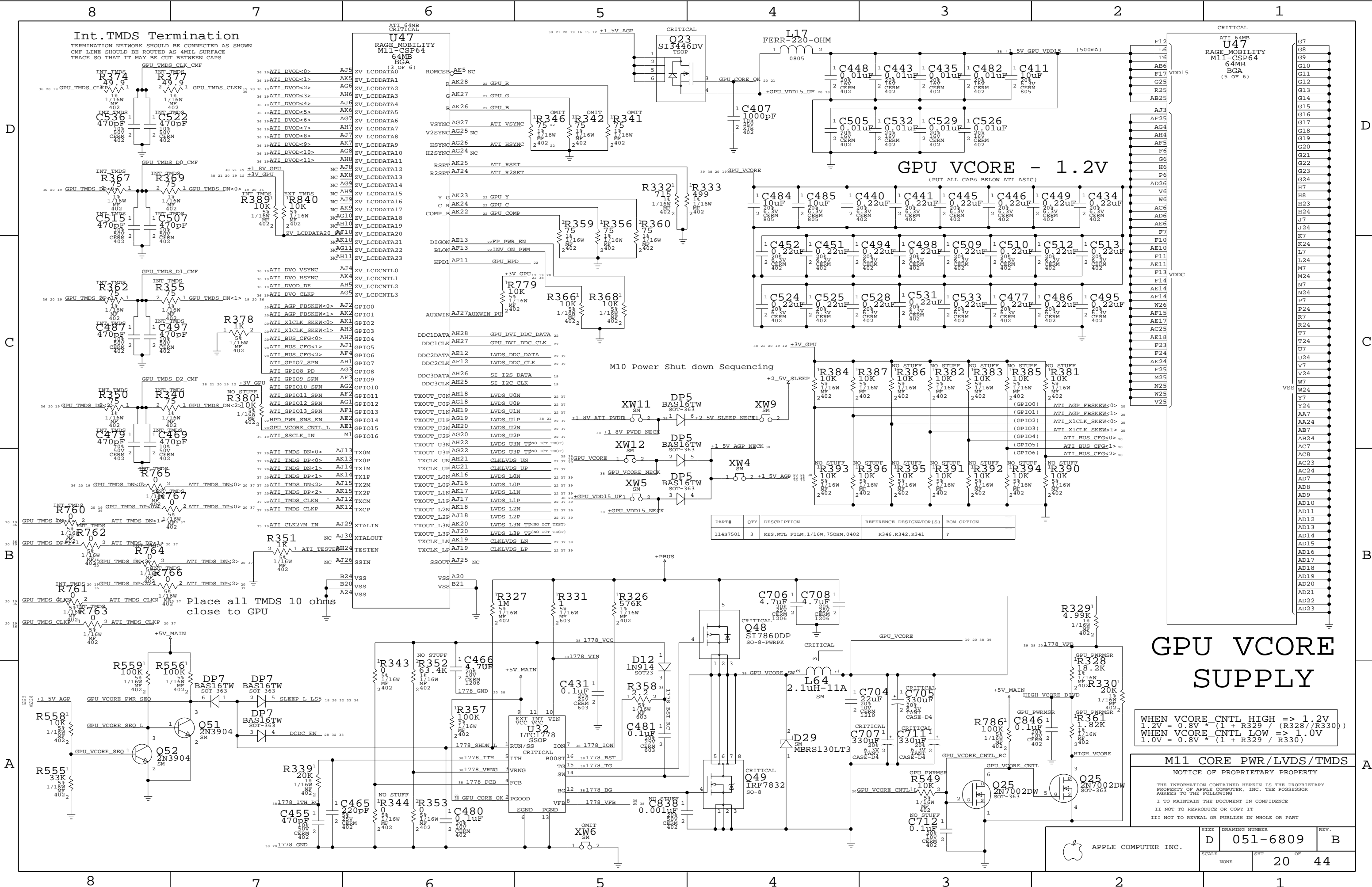
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Int.TMDS Termination
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMP LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU VCORE - 1.2V
(PUT ALL CAPS BELOW ATT ASIC)

M10 Power Shut down Sequencing

Place all TMDS 10 ohms
close to GPU

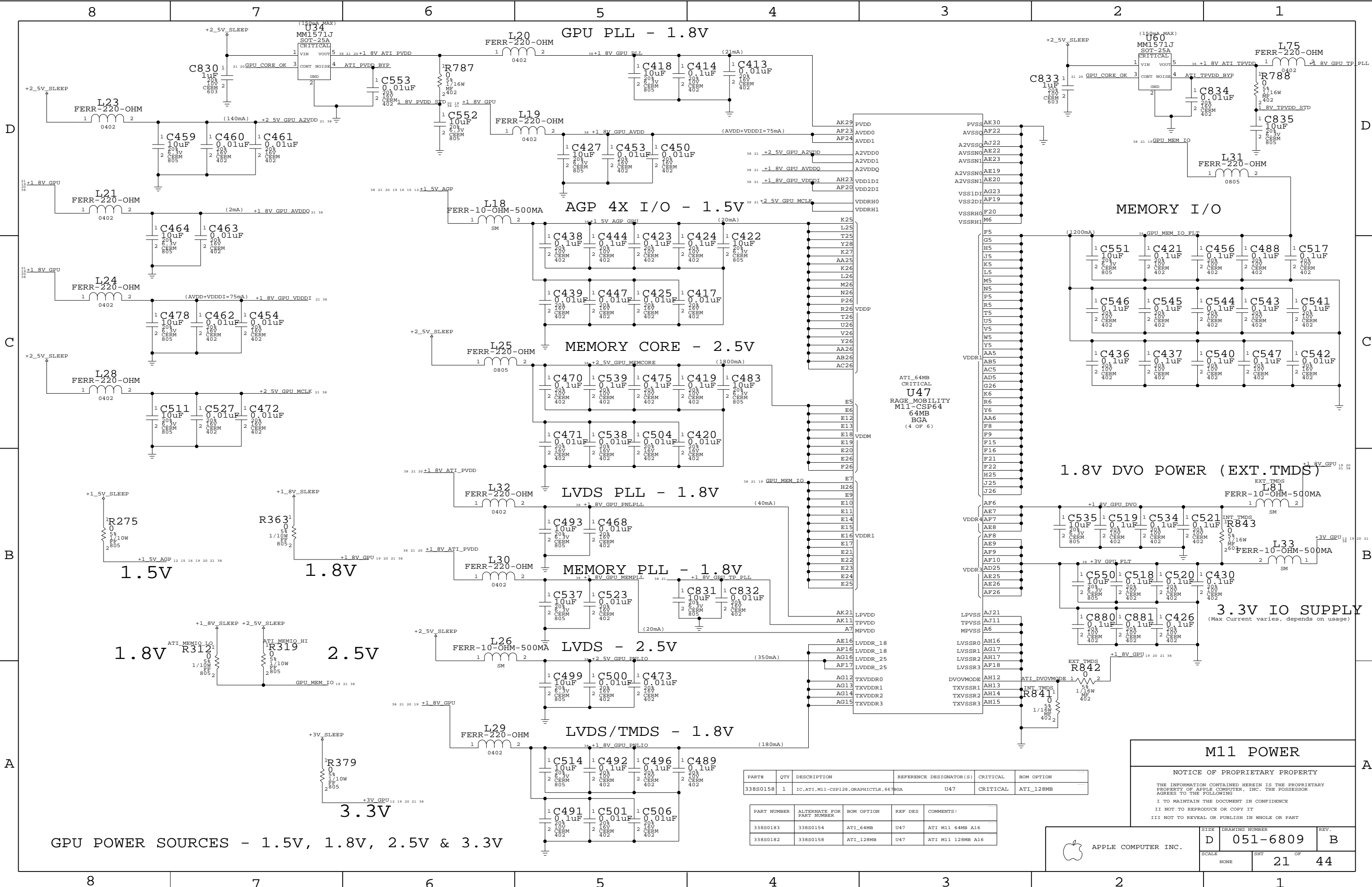
GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
 $1.2V = 0.8V * (1 + R329 / (R328 // R330))$
WHEN VCORE_CNTL LOW => 1.0V
 $1.0V = 0.8V * (1 + R329 / R330)$

M11 CORE PWR/LVDS/TMDS

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11487501	3	RES,MTL FILM,1/16W,75OHM,0402	R346,R342,R341	?



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRAPHICCTLR,667BGA	U47	CRITICAL	ATI_128MB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0183	338S0154	ATI_64MB	U47	ATI M11 64MB A16
338S0182	338S0158	ATI_128MB	U47	ATI M11 128MB A16

M11 POWER

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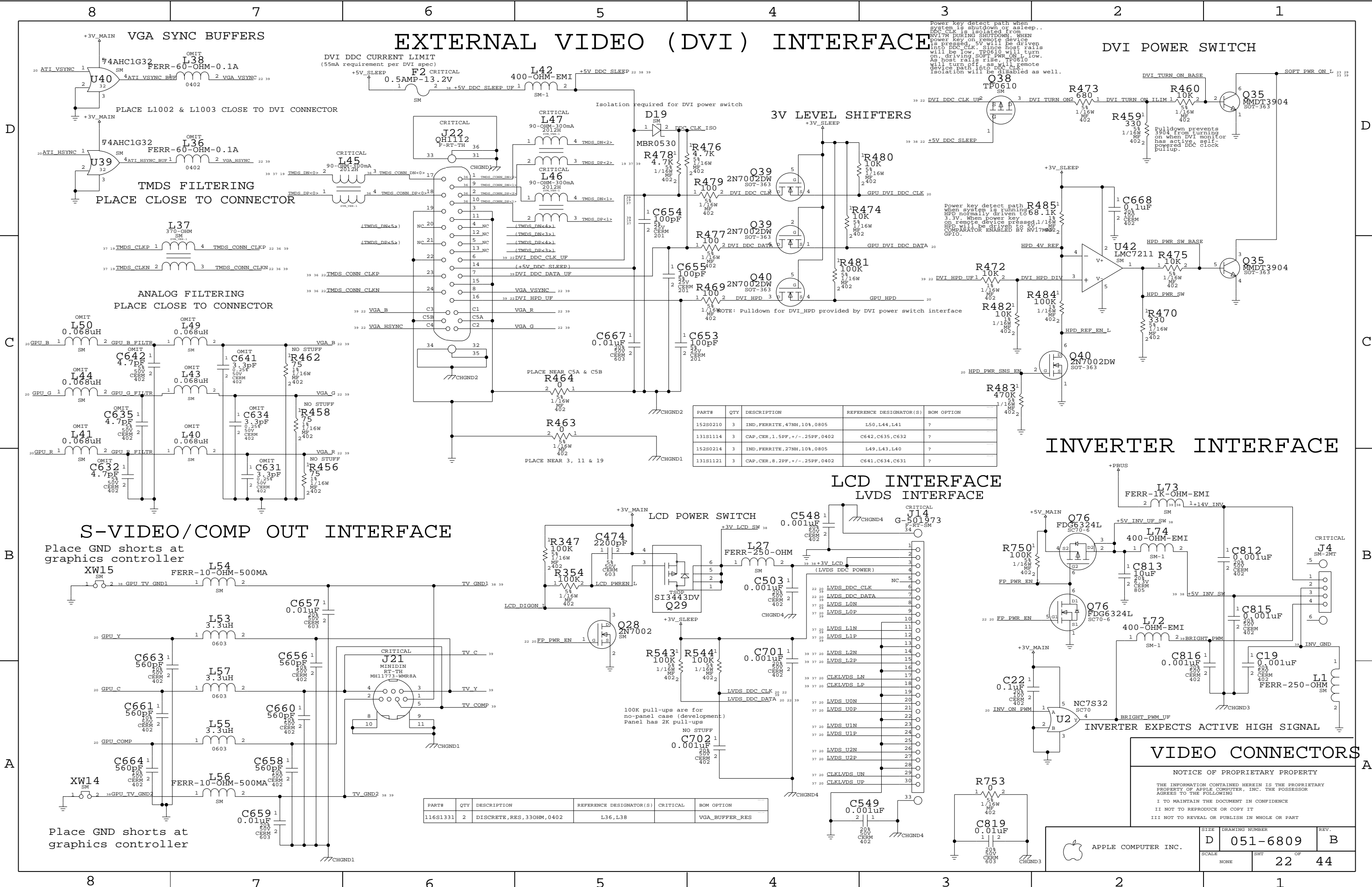
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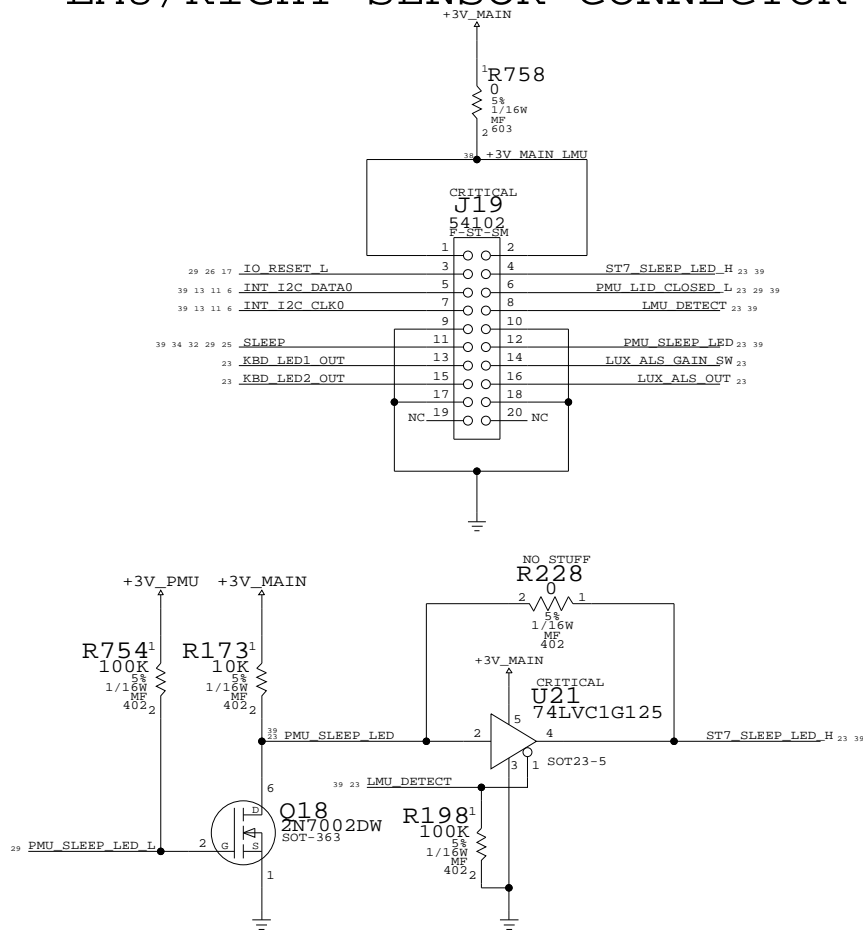
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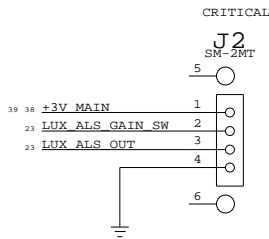
EXTERNAL VIDEO (DVI) INTERFACE



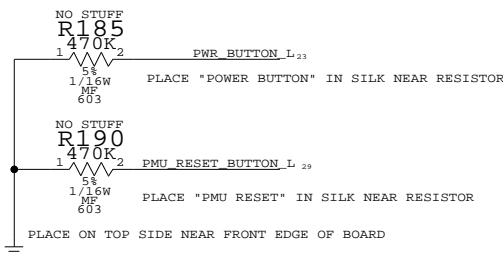
LMU/RIGHT SENSOR CONNECTOR



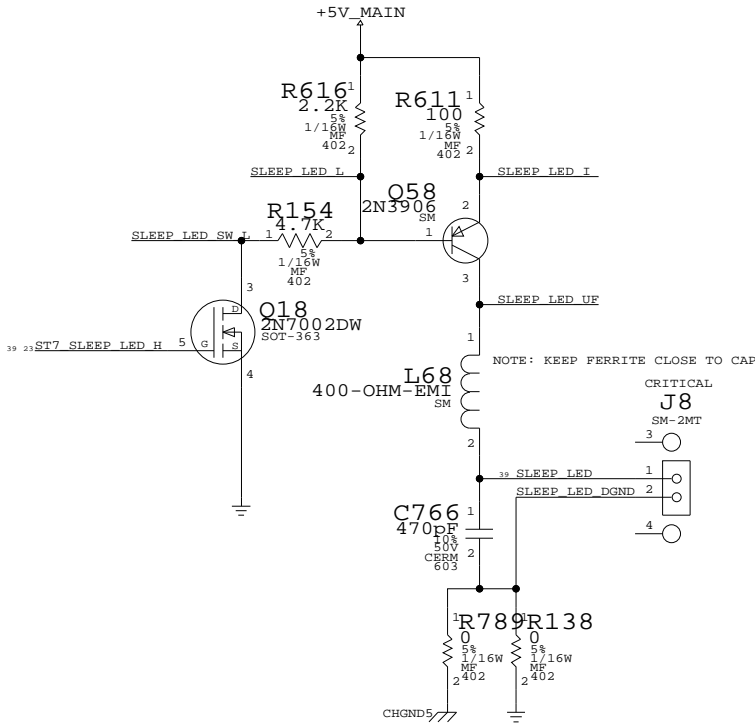
LEFT LIGHT SENSOR CONNECTOR



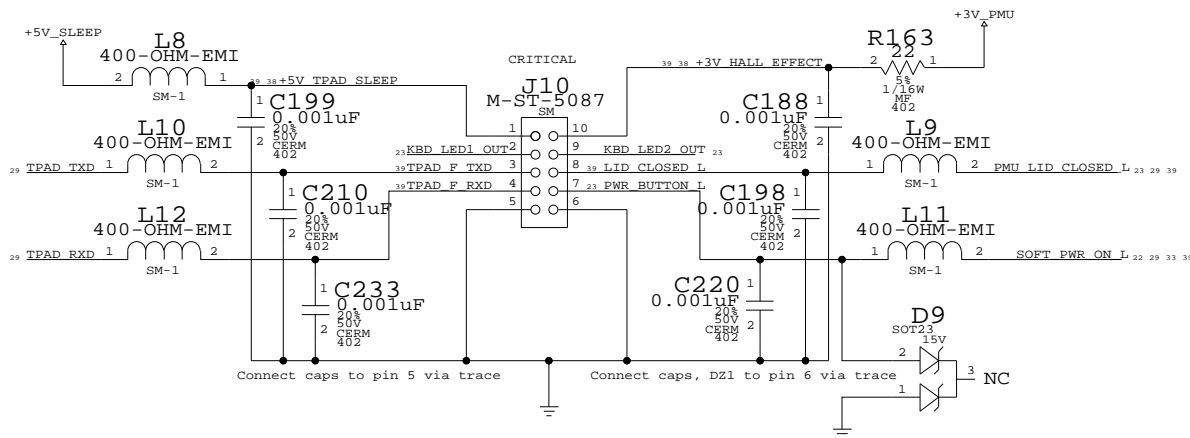
DEBUG HELPERS



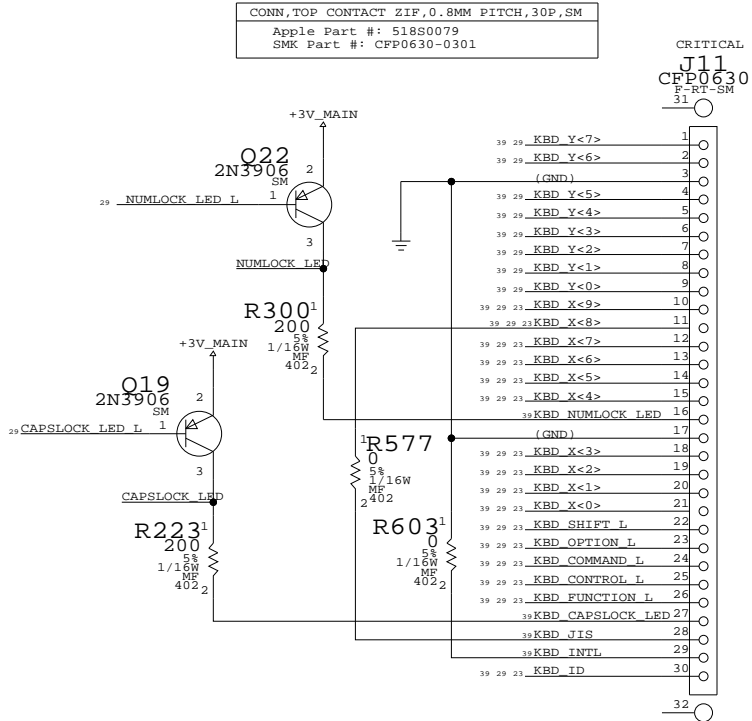
SLEEP LED



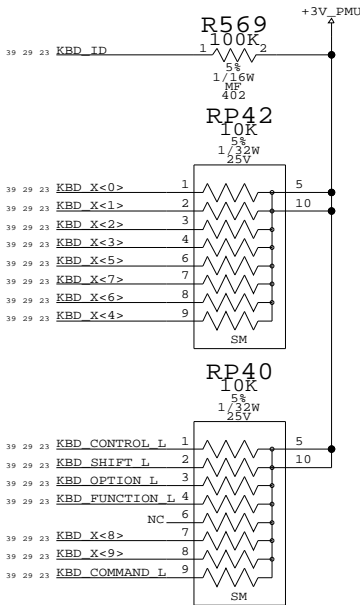
TRACKPAD/PWR BTN CONN



TOP CONTACT ZIF KEYBOARD CONN



KEYBOARD PULLUPS



KEYBOARD/TPAD/SLEEP LED

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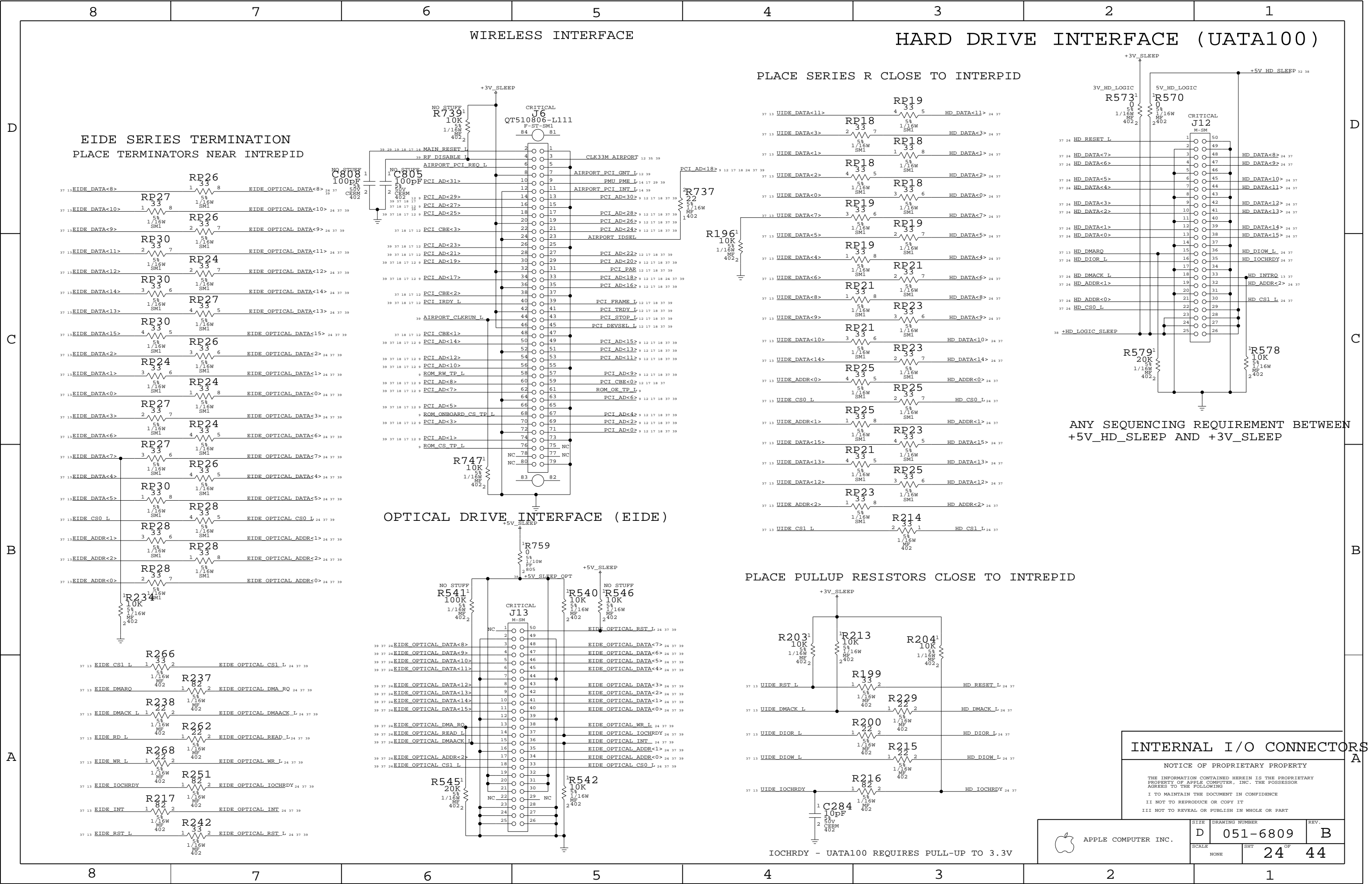
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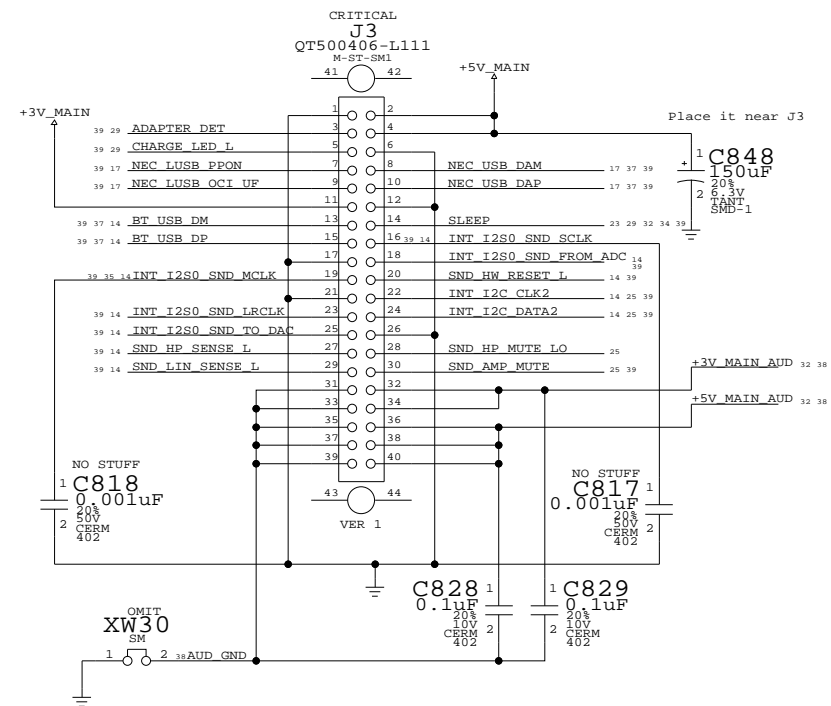


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	23	44



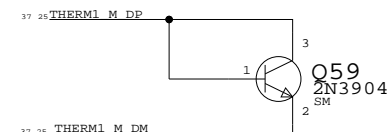
LEFT I/O & AUDIO BOARD (LIO)



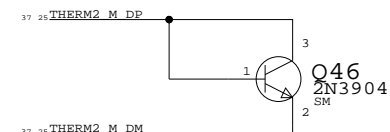
```

PLACE CLOSE TO CPU
MAIN1

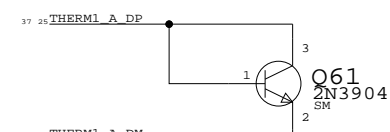
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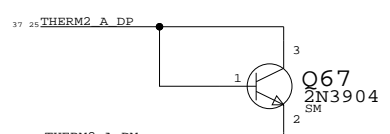
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLYTH
MAIN2



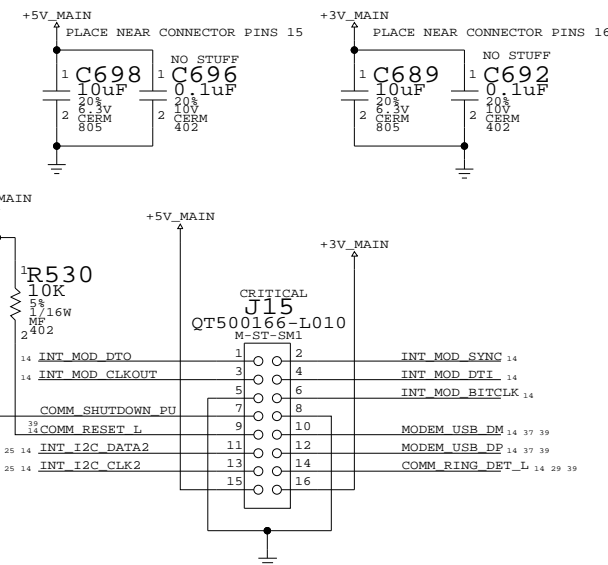
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



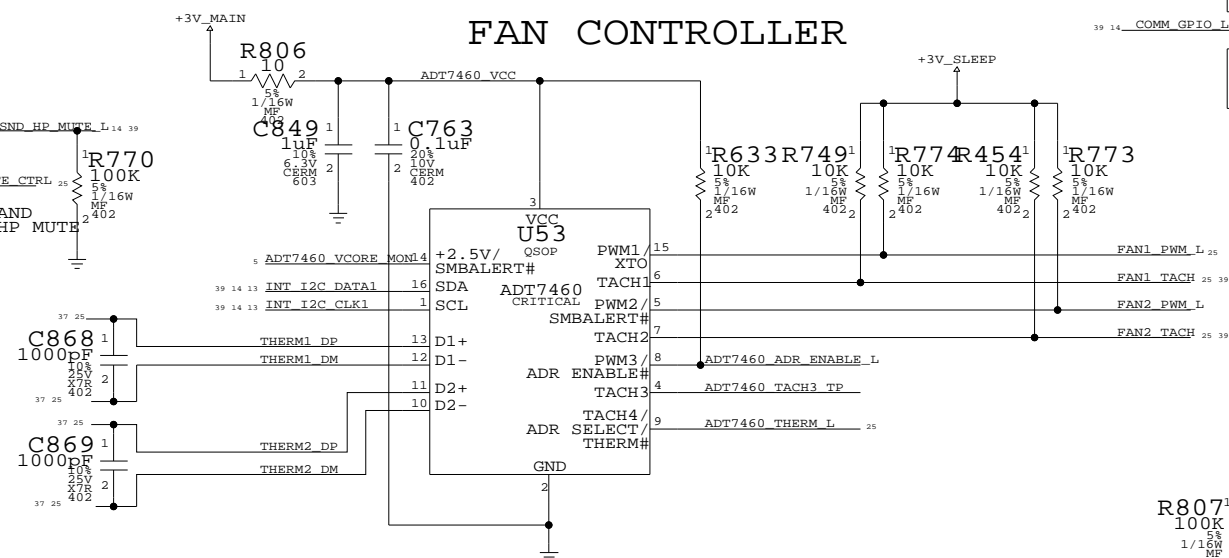
USB MODEM/SOFT MODEM RIGHT USB BOARD



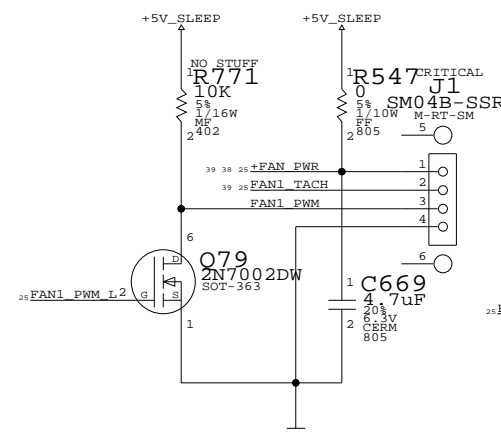
USB MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

FAN INTERFACE

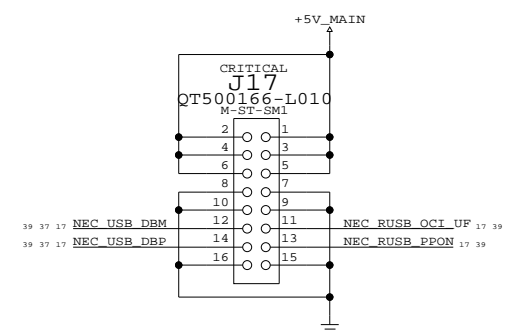
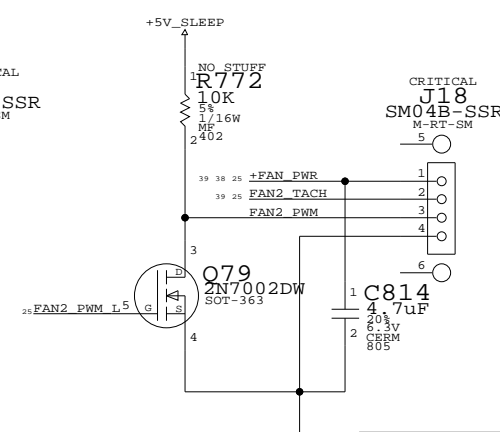
FAN CONTROLLER



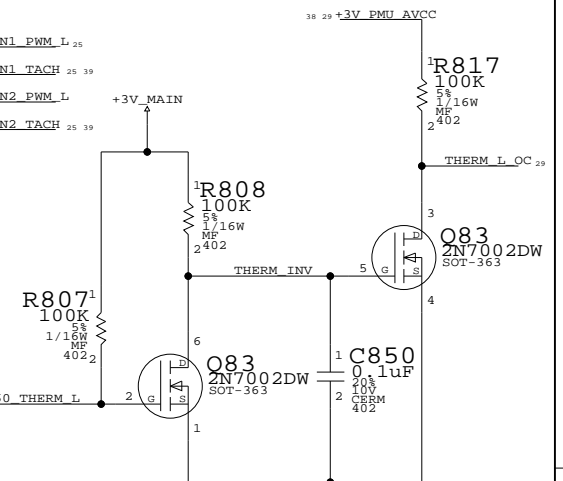
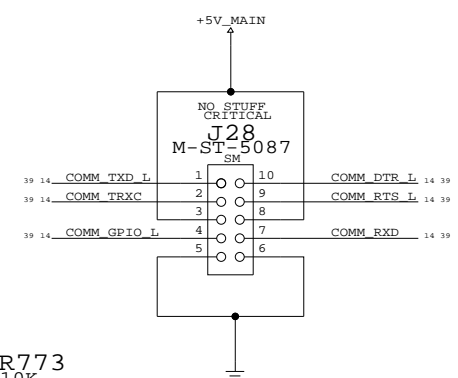
CPU FAN



GPU FAN



SERIAL DEBUG INTERFACE



FAN/MODEM/SOUND/BACKUP BATT.

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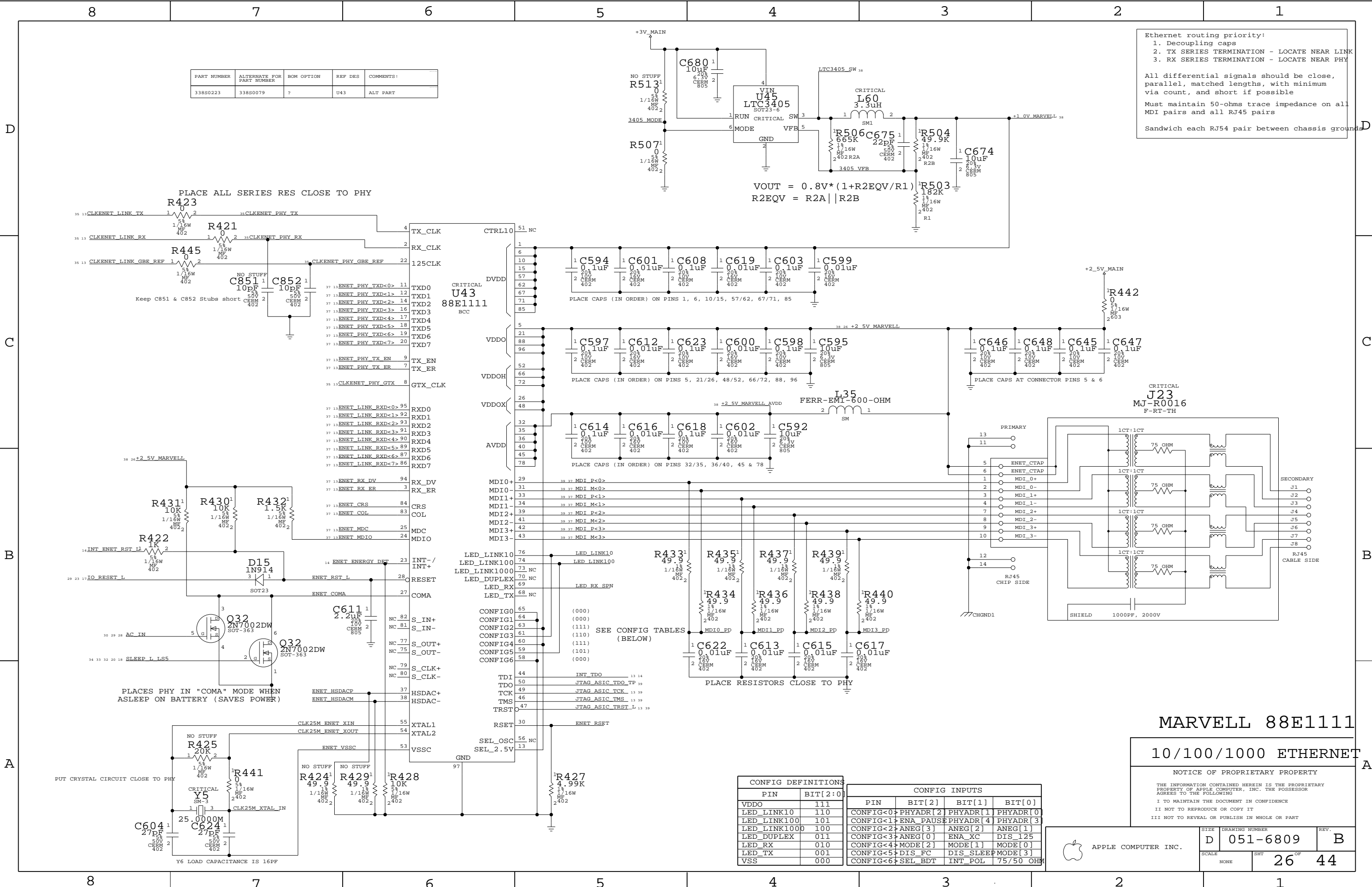
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	SIZE	DRAWING NUMBER
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-6809	REV. B
SCALE NONE	SHT 25 OF 44	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079	?	U43	ALT PART

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PLACE ALL SERIES RES CLOSE TO PHY

$$VOUT = 0.8V * (1 + R2EQV / R1)$$
$$R2EQV = R2A || R2B$$

Keep C851 & C852 Stubs short

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE RESISTORS CLOSE TO PHY

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PUT CRYSTAL CIRCUIT CLOSE TO PHY

Y6 LOAD CAPACITANCE IS 16PF

CRITICAL
U43
88E1111
BCC

CRITICAL
J23
MJ-R0016
F-RT-TH

LED_LINK10
LED_LINK100
LED_LINK1000
LED_DUPLEX
LED_RX
LED_TX
LED_RX_SPN

CONFIG0 (000)
CONFIG1 (000)
CONFIG2 (111)
CONFIG3 (110)
CONFIG4 (111)
CONFIG5 (101)
CONFIG6 (000)

INT_TDO 13 14
JTAG_ASIC_TDO_TP 39
JTAG_ASIC_TCK 13 39
JTAG_ASIC_TMS 13 39
JTAG_ASIC_TRST_L 13 39

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

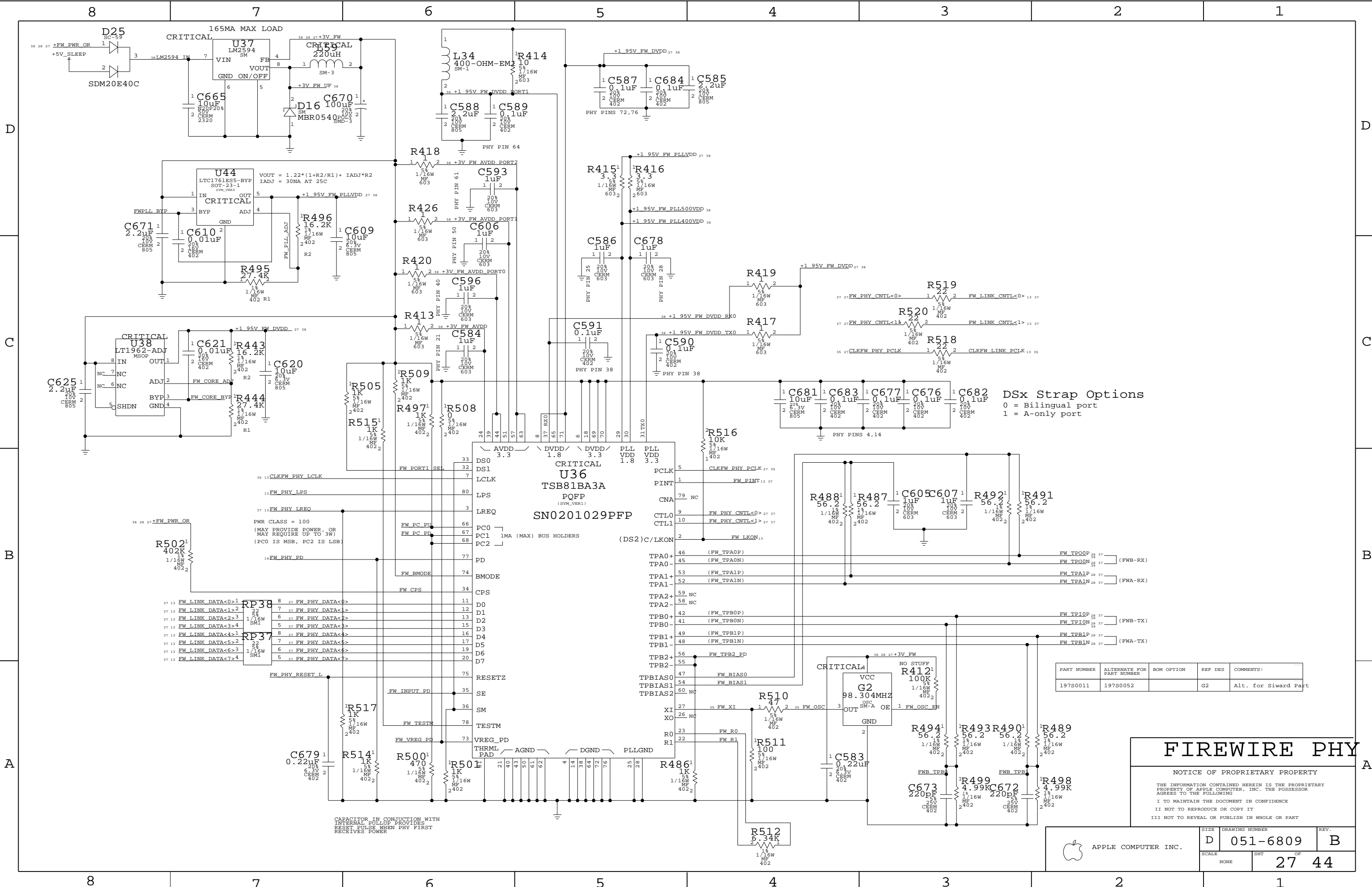
MARVELL 88E1111

10/100/1000 ETHERNET

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6809	B
SCALE	NONE	SHT	26 OF 44



DSx Strap Options

0	= Bilingual port
1	= A-only port

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052		G2	Alt. for Siward Part

FIREWIRE PHY

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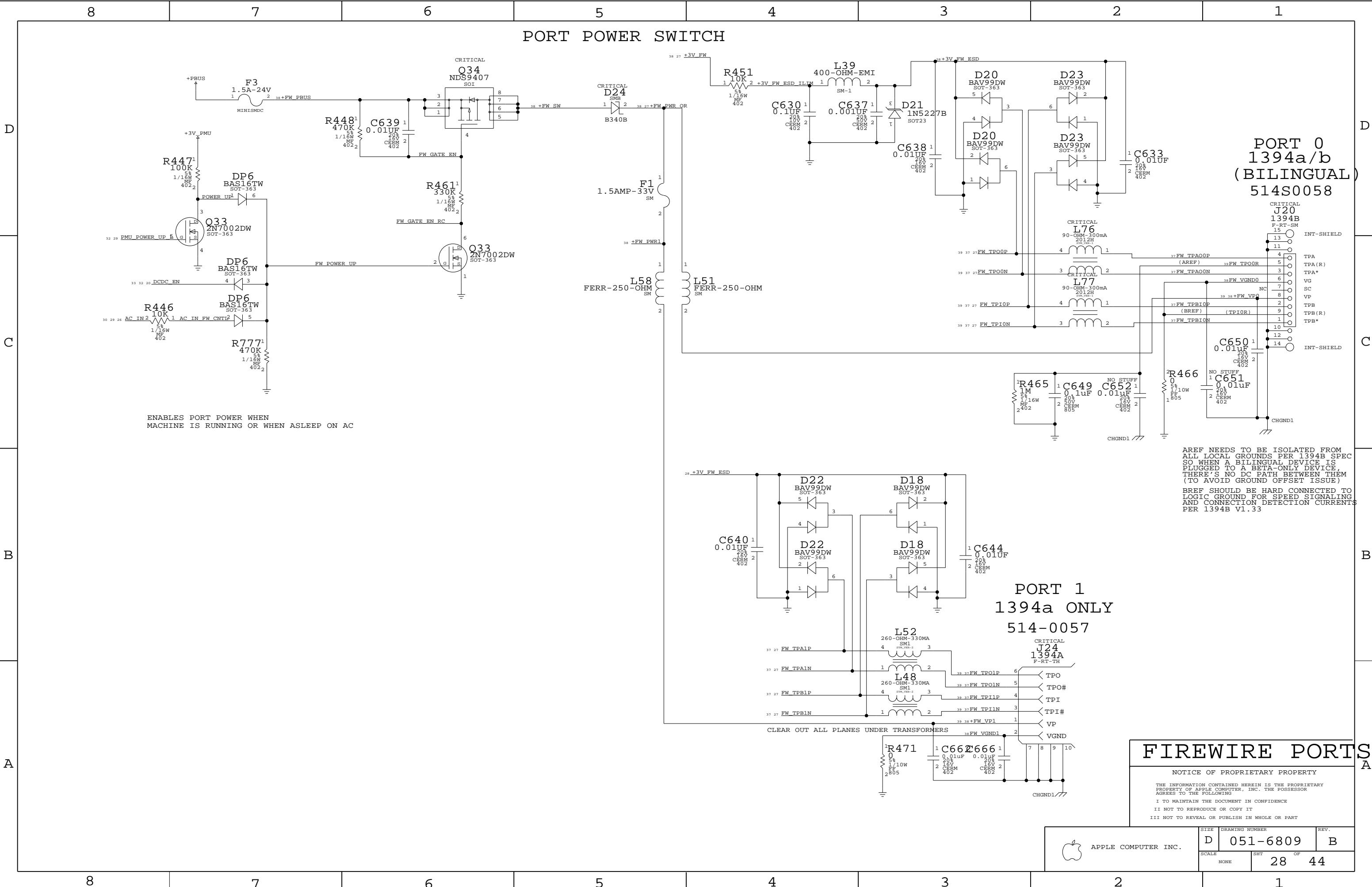
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6809	B
SCALE	NONE	SHT	OF
		27	44



PORT POWER SWITCH

PORT 0
1394a/b
(BILINGUAL)
514S0058

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO A BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)
BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

PORT 1
1394a ONLY
514-0057

FIREWIRE PORTS

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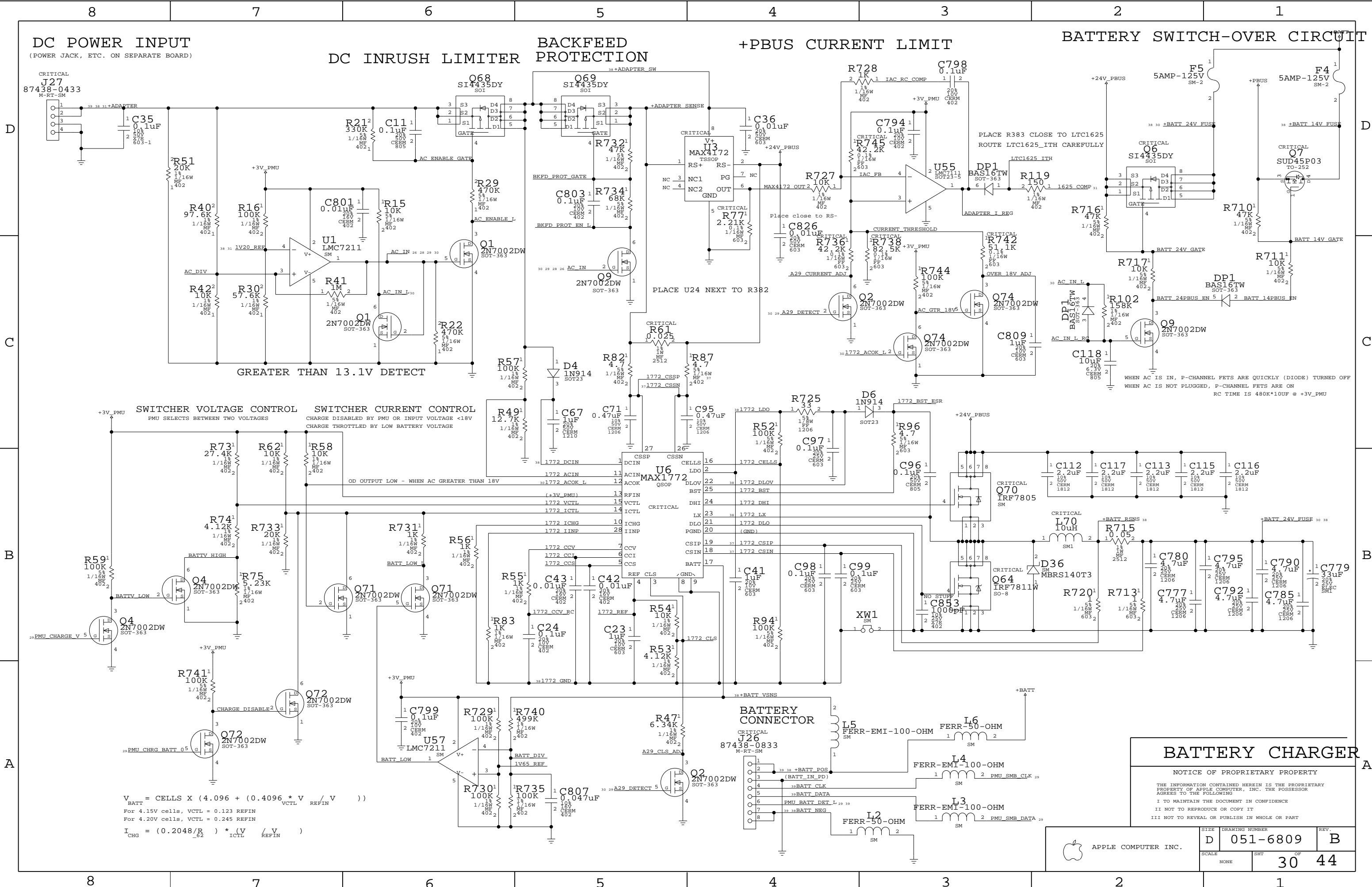
APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6809 B

SCALE SHEET OF

NONE 28 44



DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

DC INRUSH LIMITER

BACKFEED PROTECTION

+PBUS CURRENT LIMIT

BATTERY SWITCH-OVER CIRCUIT

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

BATTERY CONNECTOR

BATTERY CHARGER

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$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$$I_{CHG} = (0.2048 / R_{G2}) \times (V_{VCTL} / V_{REFIN})$$

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	30	44

D

C

B

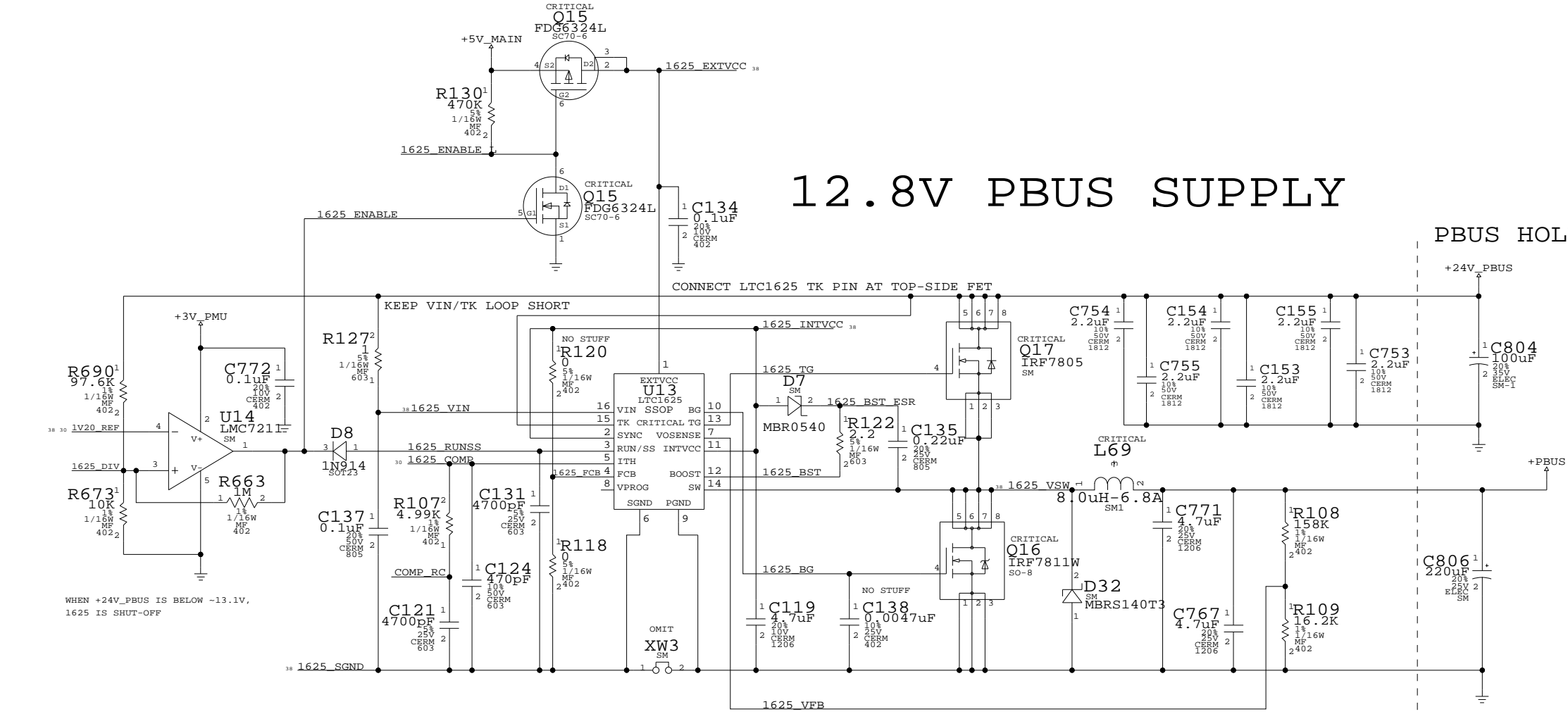
A

D

C

B

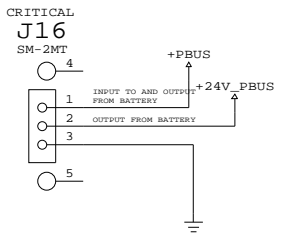
A



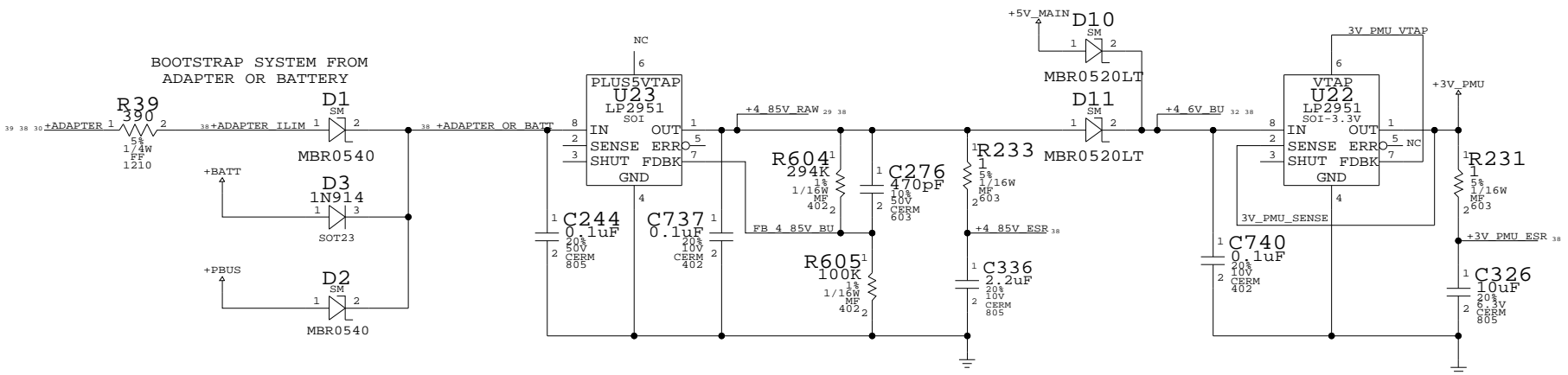
12.8V PBUS SUPPLY

PBUS HOLD-UP CAPS

BACKUP BATTERY



PMU SUPPLY



12.8V REGULATOR

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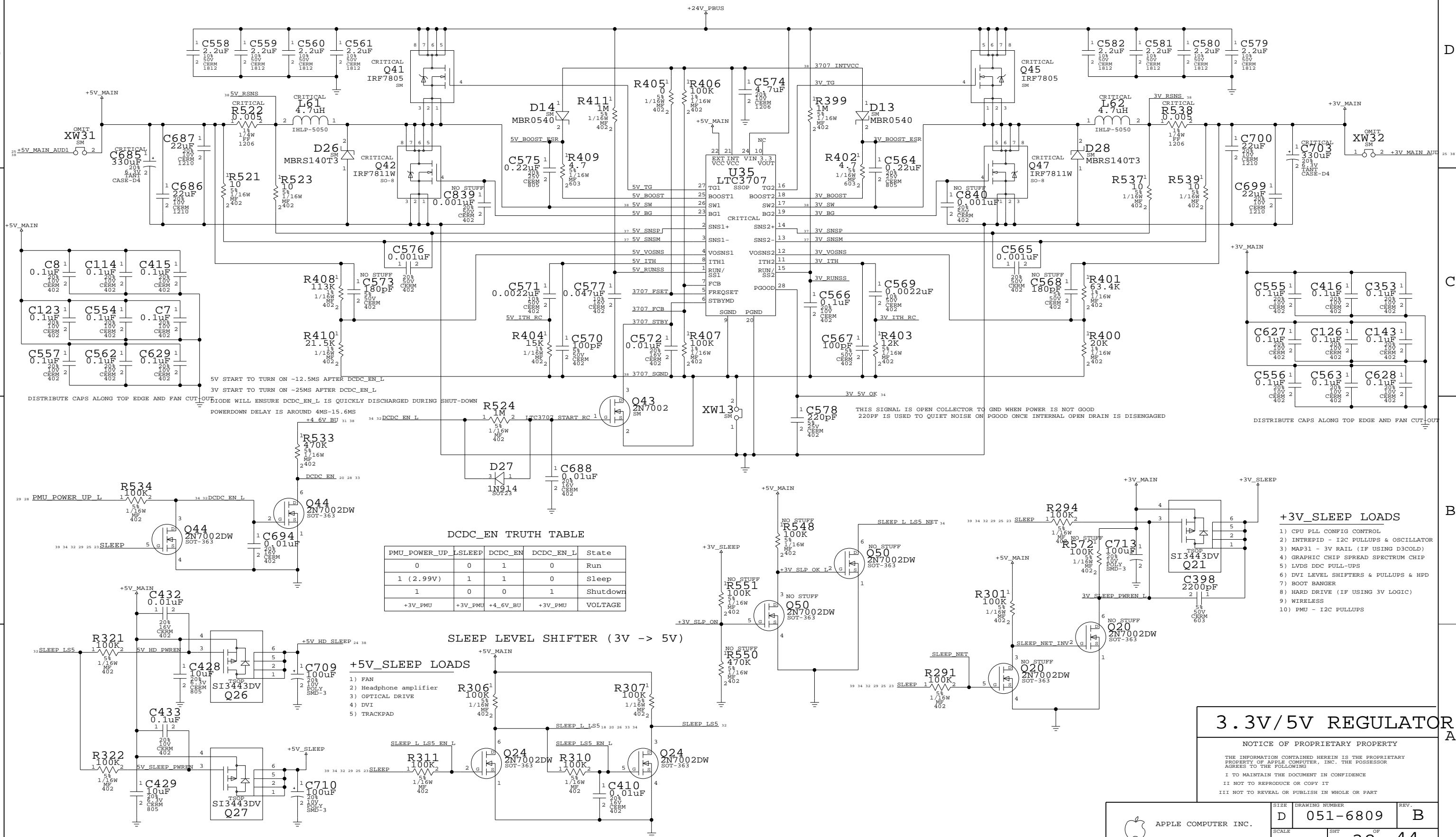
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	D	051-6809	B
SCALE	SHT		31 OF 44
	NONE		

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

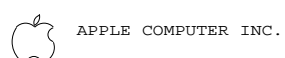
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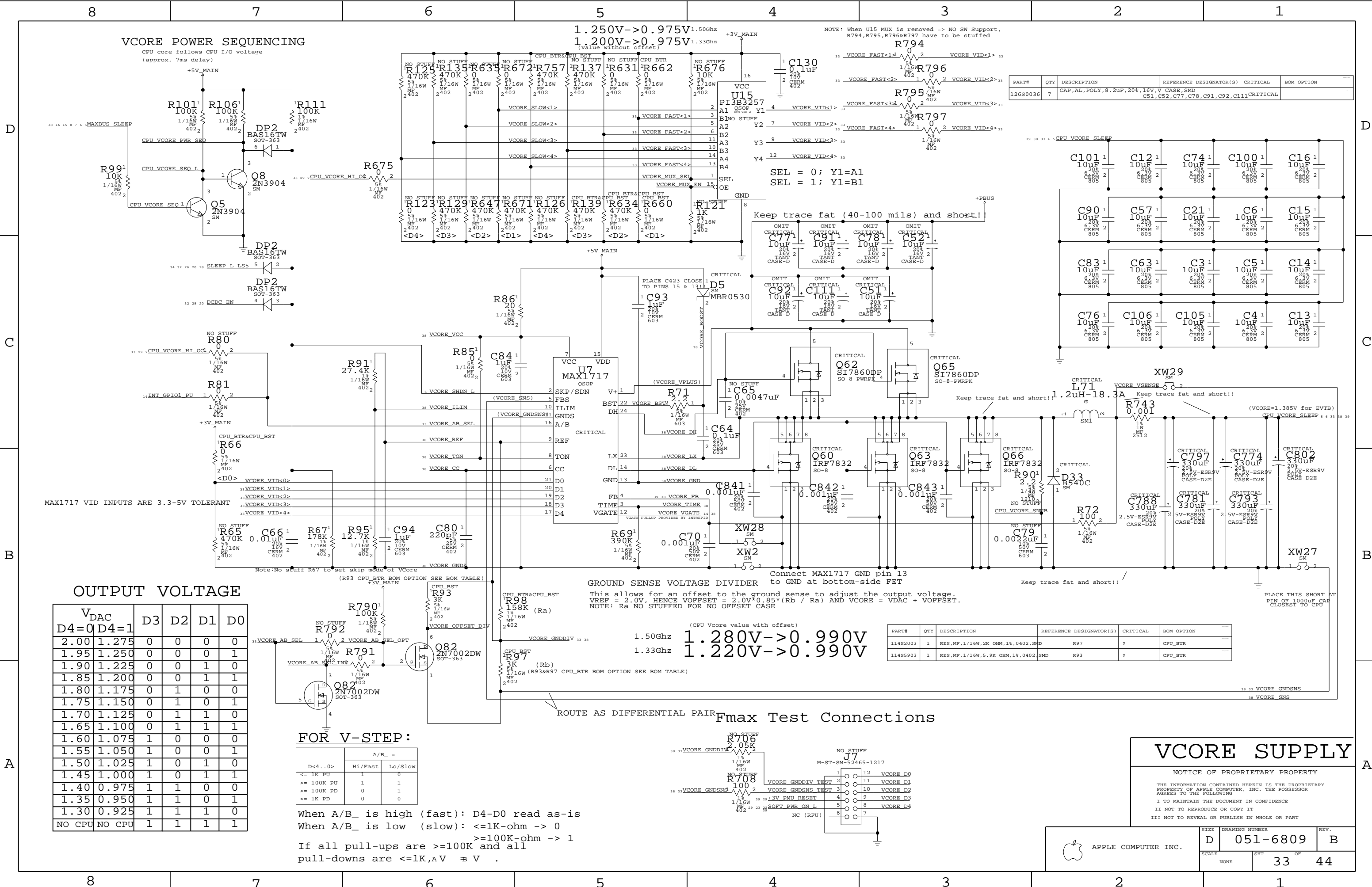
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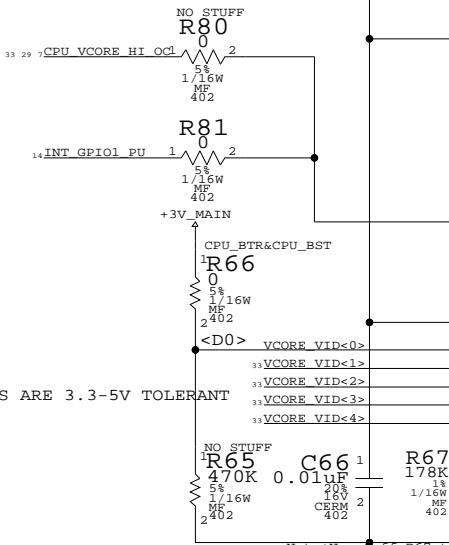
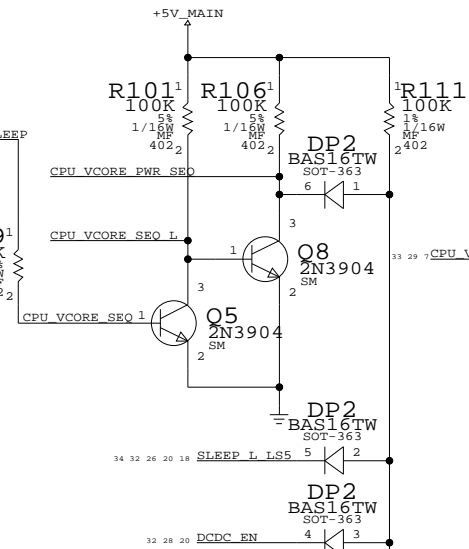


SIZE	D	DRAWING NUMBER	051-6809	REV.	B
SCALE	NONE	SHT	32	OF	44



Vcore POWER SEQUENCING

CPU core follows CPU I/O voltage (approx. 7ms delay)



MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

OUTPUT VOLTAGE

V _{DAC}		D3	D2	D1	D0
D4=0	D4=1				
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

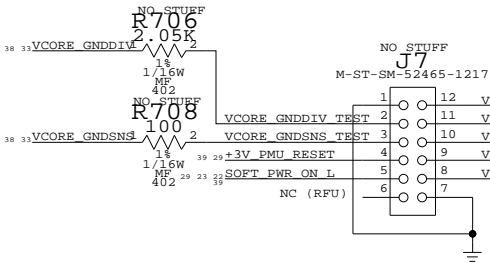
When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
=>100K-ohm -> 1
If all pull-ups are >=100K and all pull-downs are <=1K, A/V = V

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V*0.85*(Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

1.50Ghz 1.280V->0.990V
1.33Ghz 1.220V->0.990V

Fmax Test Connections



VCORE SUPPLY

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SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	33	44

1.5V/2.5V SWITCHER

+1.5V_SLEEP LOADS

- 1) AGP I/O - IF USING D3COLD
- 2) MAXBUS I/O - IF 1.5V INTERFACE

+1.5V_MAIN LOADS

- 1) INTREPID CORE

+2.5V_MAIN LOADS

- 1) MAP31 - FBCORE/FBIO IF USING D3HOT
- 2) GIGABIT ETHERNET - AVDDL
- 3) DDR SODIMMS - CORE/IO
- 4) DDR MUXES

M11 Power Shut down Sequencing

+2.5V_SLEEP LOADS

- 1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1.8V_MAIN LOADS

- 1) INTREPID PLLS

+1.8V_SLEEP LOADS

- 1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
- 2) CPU JTAG & MaxBus Pull-ups
- 3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

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SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	34	44

[illegible]

	8	7	6	5	4	3	2	1	
	Digital Signals (cont'd)								
	GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIA	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
D	AGP	AGP AD<15..0>	L:S:1050:1450	7					66 MHz
	AGP BYTES 0-1	AGP CB<1..0>	L:S:1050:1450	7					66 MHz
		AGP AD STB<0>	L:S:1050 MTL:1450 MTL			(250)	8 MIL SPACING		133.0 MHz
	AGP BYTES 2-3	AGP AD STB L<0>	L:S:1050 MTL:1450 MTL			(250)	8 MIL SPACING		133.0 MHz
		AGP AD<31..16>	L:S:1050:1450	7					66 MHz
		AGP CB<3..2>	L:S:1050:1450	7					66 MHz
	AGP SIDEBAND	AGP AD STB<1>	L:S:1050 MTL:1450 MTL			(250)	8 MIL SPACING		133.0 MHz
		AGP AD STB L<1>	L:S:1050 MTL:1450 MTL			(250)	8 MIL SPACING		133.0 MHz
		AGP SB<7..0>	L:S:1050:1450	7					66 MHz
		AGP SB STB	L:S:1050 MTL:1450 MTL			(350)	8 MIL SPACING		66.00 MHz
		AGP SB STB L	L:S:1050 MTL:1450 MTL			(350)	8 MIL SPACING		66.00 MHz
	AGP CONTROL	AGP FRAME L	L:S:1250 MTL:1950 MTL						66.00 MHz
		AGP IRDY L	L:S:1250 MTL:1950 MTL						66.00 MHz
		AGP TRDY L	L:S:1250 MTL:1950 MTL						66.00 MHz
		AGP DEVSEL L	L:S:1250 MTL:1950 MTL						66.00 MHz
		AGP STOP L	L:S:1250 MTL:1950 MTL						66.00 MHz
		AGP PAR	L:S:1250 MTL:1950 MTL						66.00 MHz
		AGP REQ L	L:S:1250 MTL:1950 MTL						66.00 MHz
		AGP GNT L	L:S:1250 MTL:1950 MTL						66.00 MHz
		AGP RBF L	L:S:1250 MTL:1950 MTL						66.00 MHz
C	PCI	PCI AD<31..0>	L:S:6000:12500				MIN DAISY CHAIN		33 MHz
		PCI CB<3..0>	L:S:6000:12500				MIN DAISY CHAIN		33 MHz
		PCI FRAME L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHz
		PCI IRDY L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHz
		PCI TRDY L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHz
		PCI DEVSEL L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHz
		PCI STOP L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHz
		PCI PAR	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHz
B	ULTRA ATA-10	UIDE DATA<15..8>	L:S:710			(200)			100 MHz
		UIDE DATA<7>	U51:V1:RP19:3:600 MTL			(200)			100.0 MHz
		UIDE DATA<6..0>	L:S:600			(200)			100 MHz
		UIDE ADDR<2..0>	L:S:650			(200)	NEED TO MATCH DELAY TO 250		100 MHz
		UIDE RST L	L:S:400 MTL			(200)			100.0 MHz
		UIDE DIOW L	L:S:400 MTL			(200)			100.0 MHz
		UIDE DIOR L	L:S:600 MTL			(200)			100.0 MHz
		UIDE DMACK L	L:S:400 MTL			(200)			100.0 MHz
		UIDE CS0 L	L:S:500 MTL			(200)			100.0 MHz
		UIDE CS1 L	L:S:500 MTL			(200)			100.0 MHz
		UIDE DMARQ	L:S:400 MTL			(200)			100.0 MHz
		UIDE IOCHRDY	L:S:600 MTL			(200)			100.0 MHz
		UIDE INTRO	L:S:400 MTL			(200)			100.0 MHz
		HD DATA<15..0>	L:S:5000:6500	7		(200)			100 MHz
		HD ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHz
		HD RESET L	L:S:4000 MTL:6000 MTL			(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHz
		HD DIOW L	L:S:3000 MTL:520						

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND
LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
SCAN/TEST	JTAG ASIC TMS	TRUE		13 26
	JTAG ASIC TDI	TRUE		13
	JTAG ASIC TDO_TP	TRUE		26
	JTAG ASIC TCK	TRUE		13 26
	JTAG ASIC TRST L	TRUE		13 26
	CPU_CHKSTP_OUT_L	TRUE		5
	CPU_SRESET_L	TRUE		5
	CPU_HRESET_L	TRUE		5 6 7
	JTAG_CPU_TMS	TRUE		5 6
	JTAG_CPU_TDI	TRUE		5 6
	JTAG_CPU_TDO_TP	TRUE		5
	JTAG_CPU_TCK	TRUE		5 6
	JTAG_CPU_TRST_L	TRUE		5 6
	INT_JTAG_TEI	TRUE		13
	INT_TST_MONIN_PD	TRUE		13
	INT_TST_MONOUT_TP	TRUE		13
	INT_TST_PLEN_PD	TRUE		13
	INT_I2C_CLK0	TRUE		6 11 13 23
	INT_I2C_DATA0	TRUE		6 11 13 23
	INT_I2C_CLK1	TRUE		13 14 25
INT I2C	INT_I2C_DATA1	TRUE		13 14 25
	+PBUS	TRUE		38
PWR/GND	+24V_PBUS	TRUE		38
	GPU_VCORE	TRUE		19 20 38
	1778_VFB	TRUE		20 38
	CPU_VCORE_SLEEP	TRUE		5 6 33 38
	VCORE_FB	TRUE		23 38
	+1.8V_MAIN	TRUE		38
	+2.5V_MAIN	TRUE		38
	+5V_MAIN	TRUE	2	38 39
	+5V_SLEEP	TRUE	2	38 39
	+3V_MAIN	TRUE	4	23 38
	+3V_PMU	TRUE		38
	CBUS_DET_1_L	TRUE		2000
CARDBUS DVI	CBUS_DET_2_L	TRUE		2000
	TMDS_DM<0..2>	TRUE		1000
	TMDS_DP<0..2>	TRUE		1000
	TMDS_CONN_CLKN	TRUE		1000
	TMDS_CONN_CLKP	TRUE		1000
	VGA_R	TRUE		1000
	VGA_G	TRUE		1000
	VGA_B	TRUE		1000
	VGA_HSYNC	TRUE		1000
	VGA_VSYNC	TRUE		1000
	DVI_DDC_CLK_UF	TRUE		1000
	DVI_DDC_DATA_UF	TRUE		1000
LVDS	DVI_HPD_UF	TRUE		1000
	+5V_DDC_SLEEP	TRUE		2000
	CHGND1	TRUE	2	2000
	CHGND1	TRUE	6	1000
	LVDS_L0N	TRUE		1000
	LVDS_L0P	TRUE		1000
	LVDS_L1N	TRUE		1000
	LVDS_L1P	TRUE		1000
	LVDS_L2N	TRUE		1000
	LVDS_L2P	TRUE		1000
	CLKLVDS_LN	TRUE		1000
	CLKLVDS_LP	TRUE		1000
INVERTER	LVDS_DDC_CLK	TRUE		1000
	LVDS_DDC_DATA	TRUE		1000
	+3V_LCD	TRUE	2	2000
	+3V_SLEEP	TRUE		2000
	CHGND4	TRUE	2	2000
	CHGND4	TRUE	6	1000
	+14V_INV	TRUE		2000
	+5V_INV_SW	TRUE		2000
	BRIGHT_PWM	TRUE		2000
	INV_GND	TRUE		2000
	TV_C	TRUE		2000
	TV_Y	TRUE		2000
S-VIDEO	TV_COMP	TRUE		2000
	TV_GND1	TRUE		2000
	TV_GND2	TRUE		2000
	INT_I2S0_SND_TO_DAC	TRUE		1000
	INT_I2S0_SND_LRCLK	TRUE		1000
	INT_I2S0_SND_MCLK	TRUE		1000
	INT_I2S0_SND_SCLK	TRUE		1000
	INT_I2S0_SND_FROM_ADC	TRUE		1000
	SND_HP_MUTE_L	TRUE		1000
	SND_HP_MUTE	TRUE		1000
	SND_HW_RESET_L	TRUE		1000
	SND_HP_SENSE_L	TRUE		1000
L1O	SND_LIN_SENSE_L	TRUE		1000
	INT_I2C_CLK2	TRUE		1000
	INT_I2C_DATA2	TRUE		1000
	ADAPTER_DET	TRUE		1000
	CHARGE_LED_L	TRUE		1000
	NEC_LUSB_OCI_UF	TRUE		1000
	NEC_LUSB_PPON	TRUE		1000
	+5V_MAIN	TRUE	2	2000
	+5V_SLEEP	TRUE	2	2000
	+3V_SLEEP	TRUE		2000
	+3V_SLEEP	TRUE		2000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
USB	NEC_USB_DAM	TRUE		17 25 37
	NEC_USB_DAP	TRUE		17 25 37
	NEC_USB_DBM	TRUE		17 25 37
	NEC_USB_DBP	TRUE		17 25 37
	BT_USB_DM	TRUE		14 25 37
	BT_USB_DP	TRUE		14 25 37
	MODEM_USB_DM	TRUE		14 25 37
	MODEM_USB_DP	TRUE		14 25 37
	NEC_RUSB_PPON	TRUE		17 25
	NEC_RUSB_OCI_UF	TRUE		17 25
	PCI_AD<0..31>	TRUE		1000
	PCI_FRAME_L	TRUE		1000
	PCI_TRDY_L	TRUE		1000
	PCI_IRDY_L	TRUE		1000
	PCI_DEVSEL_L	TRUE		1000
	PCI_STOP_L	TRUE		1000
	PCI_PAR	TRUE		1000
	AIRPORT_PCI_REQ_L	TRUE		1000
	AIRPORT_PCI_GNT_L	TRUE		1000
	AIRPORT_PCI_INT_L	TRUE		1000
RT. USB WIRELESS	MAIN_RESET_L	TRUE		1000
	CLK33M_AIRPORT	TRUE		1000
	PMU_PME_L	TRUE		1000
	ROM_ONBOARD_CS_L	TRUE		1000
	ROM_OE_L	TRUE		1000
	ROM_CS_L	TRUE		1000
	ROM_RW_L	TRUE		1000
	RF_DISABLE_L	TRUE		1000
	AIRPORT_CLKRUN_L	TRUE		1000
	+3V_AIRPORT	TRUE		1000
	CHGND3	TRUE	6	1000
OPTICAL	EIDE_OPTICAL_DATA<0..15>	TRUE		2000
	EIDE_OPTICAL_DMA_RQ	TRUE		2000
	EIDE_OPTICAL_READ_L	TRUE		2000
	EIDE_OPTICAL_DMAACK_L	TRUE		2000
	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000
	EIDE_OPTICAL_CS0_L	TRUE		2000
	EIDE_OPTICAL_CS1_L	TRUE		2000
	EIDE_OPTICAL_RST_L	TRUE		2000
	EIDE_OPTICAL_WR_L	TRUE		2000
	EIDE_OPTICAL_IOCHRDY	TRUE		2000
	EIDE_OPTICAL_INT	TRUE		2000
TRACKPAD	+5V_TPAP_SLEEP	TRUE		3000
	TPAD_F_TXD	TRUE		3000
	TPAD_F_RXD	TRUE		3000
	LID_CLOSED_L	TRUE		3000
	+3V_HALL_EFFECT	TRUE		3000
	SOFT_PWR_ON_L	TRUE		3000
	COMM_RESET_L	TRUE		4000
	COMM_SHUTDOWN	TRUE		4000
	COMM_RING_DET_L	TRUE		4000
	COMM_TXD_L	TRUE		4000
MODEM/ SERIAL	COMM_TRXC	TRUE		4000
	COMM_GPIO_L	TRUE		4000
	COMM_DTR_L	TRUE		4000
	COMM_RTS_L	TRUE		4000
	COMM_RXD	TRUE		4000
KEYBOARD	KBD_ID	TRUE		3000
	KBD_INTL	TRUE		3000
	KBD_JIS	TRUE		3000
	KBD_CAPSLOCK_LED	TRUE		3000
	KBD_NUMLOCK_LED	TRUE		3000
	KBD_FUNCTION_L	TRUE		3000
	KBD_COMMAND_L	TRUE		3000
	KBD_OPTION_L	TRUE		3000
	KBD_CONTROL_L	TRUE		3000
	KBD_SHIFT_L	TRUE		3000
BATTERY	KBD_X<0..9>	TRUE		3000
	KBD_Y<0..7>	TRUE		3000
	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_CLK	TRUE		1000
	BATT_DATA	TRUE		1000
	PMU_BATT_DET_L	TRUE		1000
FANS	+FAN_PWR	TRUE		3000
	FAN1_TACH	TRUE		3000
	FAN2_TACH	TRUE		3000
	FAN1_GND	TRUE		3000
	FAN2_GND	TRUE		3000
ETHERNET	MDI_P<0..3>	TRUE		1000
	MDI_M<0..3>	TRUE		1000
FIREWIRE	FW_TP00P	TRUE		1000
	FW_TP00N	TRUE		1000
	FW_TP00R	TRUE		1000
	FW_TP10P	TRUE		1000
	FW_TP10N	TRUE		1000
	+FW_VP0	TRUE		1000
	FW_VGND	TRUE		1000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
FIREWIRE (CONT.)	FW_TP01P	TRUE		1000
	FW_TP01N	TRUE		1000
	FW_TP11P	TRUE		1000
	FW_TP11N	TRUE		1000
	+FW_VP1	TRUE		1000
	FW_VGND	TRUE		1000
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000
	CHGND2			
LMU/ALS	ST7_SLEEP_LED_H	TRUE		23
	PMU_SLEEP_LED	TRUE		23
	PMU_LID_CLOSED_L	TRUE		23 29
	LMU_DETECT	TRUE		23
MISC.	CHGND5		6	1000
	(100 MIL PROBE PREFERRED)			
	SLEEP_LED	TRUE		23
	PMU_KB_RESET_L	TRUE		29
	SLEEP	TRUE		23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE		6 29
	BB_RESET_L	TRUE		6
	+3V_PMU_RESET	TRUE		29 33

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	39	44

REVISION HISTORY

Proto/EVT Release

```

10/2/03      1. Schematic originated from Q16 MLB
11/10/03     1. Replace U56 symbol
2             Connect OVDSENSE to MAXBUS_SLEEP
3             Modify SRWD, SRWI, and IASTVIO to IASSTVIO
4             Connect SENSE to CPU_VCORE_SLEEP (PAGE 5)
5             Connect SENSEVDD to CPU_VCORE_SLEEP
6             Connect SRWSND to GND
7             Add 4 pcs 10k ohm resistor for AMP and BootRom issue (R1,R194,R236,R271)
8             Connect MPPM to GND
9             Modify CPU_PLL control to CC_FSEL interdig rod (R450)
10            Replace U47 symbol
11            Change R478 from 2m ohm to 1m ohm
12            Change R478 from 2m ohm to 1m ohm
13            Change R478 from 2m ohm to 1m ohm
14            Change R478 from 410 ohm to 10 ohm

```

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12/01/03 - 1. Modify CPU_VCORE setting.
12/02/03 - 1. Modify CPU_BTR_CPU_VCORE VID setting
12/05/03 - 1. Add cpu AVXD LDO (page 5)
          2. Change 042 and 043 to IFR7805 (37650035)
          3. Change 047 and 042 to IFR7810 (37650104)
          4. Change 042 and 0409 to IFR7810 (37650104)
          5. Connect INT_TDO from Intrepid to Cypress Chip PD* (U31)
12/12/03 - 1. Add R468 and R601 for MAX1715 2.5v adjust
          2. Change R468 and R601 to Motorola nspec
          3. Modify LDO power sequence
12/16/03 - 1. Add 10K pull down for INT_TDO on page 13
12/17/03 - 1. Change LDO Vin from +3V_MAIN to +3V_SLEEP
          2. Connect INT_TDO from Intrepid to Marvell 88E1111(U43)
          3. Add R755,R756,R758,R759 for power rail

```

DVT Release (Rev. 02)

01/30/04 - 1. Add Soft_Modem(PinH14) 10K pull-up at J15.7 (Pg 25)
2. Add Bom Table for R97 2.21K ohm VCore Offset (Pg 33)

02/04/04 - 1. C811 change to 4.7uF per MOT A7PM requirement (Pg 33)
2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)

DVT Release (Rev. 03)

```
02/12/04 - 1. CPU VCore adjustment for V1.1 A7PM CPU (Pg 33)
           2. CPU AVDD adjustment for V1.1 A7PM CPU (Pg 5)
           3. ATI INT.TMDS termination change to 0 ohm, Qty:8 (Pg 20)
           4. AGP I/O VREF voltage divider change to both 1K ohm (Pg 12)
```

DVT Release (Rev. 04)

02/13/04 - 1. INT. TMD5 Termination change to 2* 49.9ohm = 100ohm (Pg 20)

PVT Release (Rev. A)

03/11/04 - 1. INT. TMDS Termination change to 2* 75 ohm = 150ohm (except CLK pair) (Pg 20)
2. USB series termination near NEC PHY change to 47 ohm (Pg 17)

PVT Release (Rev. A - 051-6570)

04/02/04 - 1. USB series termination near NEC PHY change to 43.2 ohm (Pg 17)

Production Release (Rev. A - 051-6653)

04/09/04 - 1. Updated to Apollo 7PM rev 1.1.1 part numbers (Pg 5)
04/09/04 - 2. Updated to production BootROM part number (Pg 9)

Production Release (Rev. B - 051-6653)

04/30/04 - 1. Updated to Fast Intrepid part for 6A ReadMacro Delay value (Pg 8-15)
04/30/04 - 2. Add ATI M11 A16 parts as alternative for A15 parts (Pg 19-21)
04/30/04 - 3. Use new VGA filter to remove ghost image on external VGA display (Pg 22)

Production Release (Rev. C - 051-6653)

05/27/04 - 1. Updated BOM : 113S0006 -> 113S1000
05/27/04 - 2. Updated BOM : 132S0020 -> 132S0100

Production Release (Rev. B - 051-6809)-- merged with 051-6808

07/07/05 - Added 338S0223 (88E1111 Rev.B1) at U43 and 338S0079 as an alternate
07/08/05 - Added 337S2913 (IC,A7PM,1.33GHz,1.18VCORE) as an option
07/08/05 - Added label for EEE:SQE
07/08/05 - Replaced 740S0006 with 740S0818 (FUSE,1.5A,24V,SMD,LF) at F3
07/19/05 - Corrected symbols for 337S2838 (MPU),132S0021 (0.47uF,10%) and 138S0511 (2.2uF,10%)

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SIZE

D

DRAWING NUMBER

051-6809

REV.

B

SCALE

SHT	
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400

4

1

NONE

1

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